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ORIGINAL RESEARCH PAPER

Baugh-Wooley Multiplier design using Multiple Control Toffoli and Multiple Control Fredkin reversible logic gates

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ABSTRACT

Most error-resilient media processing applications use multipliers as their basic building blocks. These are power-consumption and computationally intensive modules. In the existing works, several types of the multipliers were used to improve the hardware capacity, but those methods did not provide sufficient results. Therefore, in this manuscript, a Baugh-Wooley Multiplier design using Multiple Control Toffoli (MCT) and Multiple Control Fredrick gate (MCF) Reversible Logic gate (BWM-MCT-MCF) will be analyzed. Initially, Reversible Full Adder (RFA) is designed using Multiple Control Toffoli and Multiple Control Fredrick gate Reversible Logic gates. Then the proposed Reversible Full Adder is used in Baugh-Wooley Multiplier. By this, it reduces the hardware complexity with higher speed, lower area, lower power consumption. The proposed BWM-MCT-MCF multiplier is implemented in MATLAB, its performance shows lower Garbage output 22.78%, 24.88%, 20.95% compared with the existing designs, like BWM-FG-FRG, BWM-RL-TG, BWM-TG-FG respectively. Then the designed BWM-MCT-MCF is implemented using Xilinx ISE tool with the Virtex 5 device. From this, the performance of the proposed FPGA-BWM-MCT-MCF method shows lower delay 23.77%, 16.86% compared with the existing designs, like FPGA-BWM-RL-TG, FPGA-BWM-TG-FG respectively.

KEYWORDS

Baugh-Wooley Multiplier, Multiple Control Toffoli (MCT), Multiple Control Fredrick gate (MCF), reversible logic gates, Reversible Full Adder (RFA)

1. INTRODUCTION

Multiplication is an important function of arithmetic operations. High-speed multipliers are in higher demand all-time [1, 2]. Over the course of previous investigations, several energy-efficient multipliers have been successfully created [3, 4]. Reversible logic produces higher power consumption and a significant amount of energy dissipation because of information loss in standard design methods [5, 6]. The power usage and delay are critical in Digital signal processing (DSP) design and manufacturing, which are the primary design parameters of DSP devices for high-performance application [7, 8]. In the DSP application, the multiplier is critical. Depending on the multiplier circuits, certain applications, like Filtering (FIR, IIR), Fourier Transforms (FFT), and convolution are utilized. Multiplication is a common computer operation, but it is done on most processors, because it is time consuming and expensive [9–13]. There is a variety of different calculation problems that can be regulated by the speed at which they are carried out, and these are called "multiplication" [14, 15].

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The development of digital circuits in the current digital era is constrained by research into alternative nano devices to CMOS technology [15-17]. The digital chips density is naturally raised as nano devices are produced in an effort to reduce power consumption and heat dissipation by this use. A number of methods were presented previously for improving the hardware capacity of the multipliers, but no one method provided sufficient results, because of lesser speed, power consumption, count of gates, garbage output, number of quantum costs are increased [18]. To overcome these issues, this work is proposed.

In this manuscript, reversible logic gates replace the half-adders and full-adders in the multiplier structure. This design uses two Reversible gates, such as Multiple Control Toffoli and Multiple Control Fredrick gate in place of a single reversible gate. It contains additional benefits for reducing the garbage being produced, which helps reduce the overall delay and power consumed by the RG. All previous designs had conceded to unwanted outputs, unwanted inputs, associated quantum cost. This manuscript concentrates on delay, garbage output, constant input, quantum costs and power calculation parameters. The proposed Baugh-Wooley Multiplier design using Multiple Control Toffoli and Multiple Control Fredrick gate Reversible Logic gates has shaved the depth of circuits and increased the speed considerably. The delay and power requirements in the reversible multiplier design are very low compared to the existing circuit designs.

The main contributions of this work are abridged below,

- Initially, RFA is designed by MCT and MCF Reversible Logic gates.
- RFA is utilized in Baugh-Wooley Multiplier.
- By this, it reduces the hardware complexity with higher speed, lower area, lower power consumption.
- The proposed BWM-MCT-MCF Multiplier is done in MATLAB.
- The performance metrics, like Gate Constant inputs, Count, Garbage outputs, quantum cost are analyzed.
- The performance of the proposed BWM-MCT-MCF approach is analyzed with the existing designs, like Baugh-Wooley Wallace tree multiplier with new architecture using Feyman gate (FG) and Fredkin gate (FRG) reversible logic (BWM-FG-FRG) [19], multipliers design utilizing Reversible logic with Toffoli Gate (BWM-RL-TG) [20], High speed low power multipliers depending on reversible logic Toffoli Gate (TG) and Feyman gate (FG) (BWM-TG-FG) [21], respectively.
- Then the designed BWM-MCT-MCF is implemented using Xilinx ISE tool with the Virtex 5 device.
- The performance metrics, such as power, delay are examined.
- The performance of the proposed FPGA-BWM-MCT-MCF approach is analyzed with the existing designs, like multipliers design utilizing Reversible logic with Toffoli gate (FPGA-BWM-RL-TG) [20], Higher speed lower power multipliers based on reversible logic (FPGA-BWM-TG-FG) [21].

The rest of this manuscript is structured as: section 2 deliberates the recent related works, section 3 explains the proposed design, section 4 demonstrates the results with discussion, section 5 concludes this manuscript.

2. LITERATURE SURVEY

Among the numerous studies based on Baugh-Wooley multiplier design, the recent works are described here.

Raveendran et al., [19] have presented BWM tree multiplier using reversible logic. The presented method was designed with the help of RFA circuit, multiple control Feynman and Fredrick reversible gate. The performance of the presented method was examined by gate count, quantum cost, garbage output, ancilla input. But the delay was increased.

Autade et al., [20] presented a multipliers design utilizing Reversible Logic with Toffoli gates. For designing the Baugh-Wooley Multiplier, first the full adder circuit using the multiple controlled reversible gates was designed. The reversible full adder was structured by the Reversible Logic and Toffoli gates. The structured full adder was used to design the Baugh-Wooley Multiplier. The number of gate count was decreased, but delay was increased.

Barati [21] has presented a higher speed lower power multipliers depending on reversible logic methods. The Reversible Half Adder, the Reversible Full Adder, the Dual Key gate, and the Kogge Stone Adder were designed using multiple control Toffoli gate and the Feynman gate. Then the designed half adder was used to design the Baugh-Wooley. But, the power was reduced, number of gate count was increased.

Rajmohan and Maheswari [22] have presented Compact Baugh-Wooley Multiplier Utilizing Reversible Logic. To design the full adder circuit, multiple controlled Toffoli reversible gates were used. The designed 5×5 reversible multiplier cell (full adder) was useful in designing Baugh-Wooley multiplier. The 5×5 reversible multiplier cell (full adder) was used, so that the number of gate count was decreased but the hardware complexity was increased.

Gudivada and Sudha [23] have presented BWM design in quantum-dot cellular automata utilizing 1-bit full adder with power dissipation analysis depending on reversible logic gates. The quantum-dot cellular automata using 1-bit full adder was designed by logic gates for reducing the area and the number of gate count. Then the designed 1-bit full adder was employed to BWM design and the quantum costs were reduced. The gate count was reduced but the speed was decreased.

3. PROPOSED DESIGN

The Baugh-Wooley Multiplier design using Multiple Control Toffoli and Multiple Control Fredrick gate Reversible Logic gates is proposed in this manuscript. Initially, RFA is

designed utilizing MCT and MCF Reversible Logic gates. Then the proposed Reversible Full Adder is used in Baugh-Wooley Multiplier. By this, it reduces the hardware complexity with higher speed, lower area, and lower power consumption.

3.1. Reversible Full Adder design using MCT and MCF

The design of RFA is represented in Fig. 1. It consists of four inputs and four outputs, the inputs are A, B, C, 0 and the outputs are sum, carry, two garbage outputs, 0 is represented as the Ancilla inputs (constant inputs). While using these reversible gates, the delay of the architecture is decreased. The output sum and carry equations of RFA is given in equation (1 and 2).

$$Sum = A \oplus B \oplus C_{in} \tag{1}$$

$$Carry = \{(A \oplus B)C_{in}\} \oplus (AB) \tag{2}$$

The proposed RFA is used for designing the BWM. Figure 2 shows the BWM design using RFA. The RFA circuits in the Baugh Wooley Multiplier are represented in white and pink cells. The cell representation of white cell is depicted in Fig. 3 and the cell representation of pink cell is depicted in Fig. 4. In this work, two reversible multiplier cells are represented: white and pink cells. The purpose and the difference of two cells are given: inside white cell AND gate is used and inside pink cells NAND gate is used. The white cells denote multiplier cell employed for the count of 2's complement. The pink cells denote multiplier cell. Here, every cell obtains 4 inputs that are, multiplicand input (vertical-pink line), multiplier input (horizontal-green line), sum from prior cells (diagonal-black line), carry from prior cells (vertical-black line). They create 2 outputs: sum output

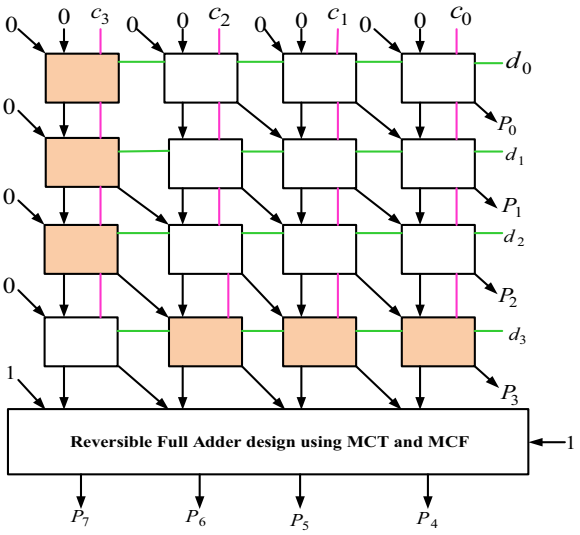

Fig. 2. Baugh-Wooley Multiplier design utilizing Reversible Full Adder

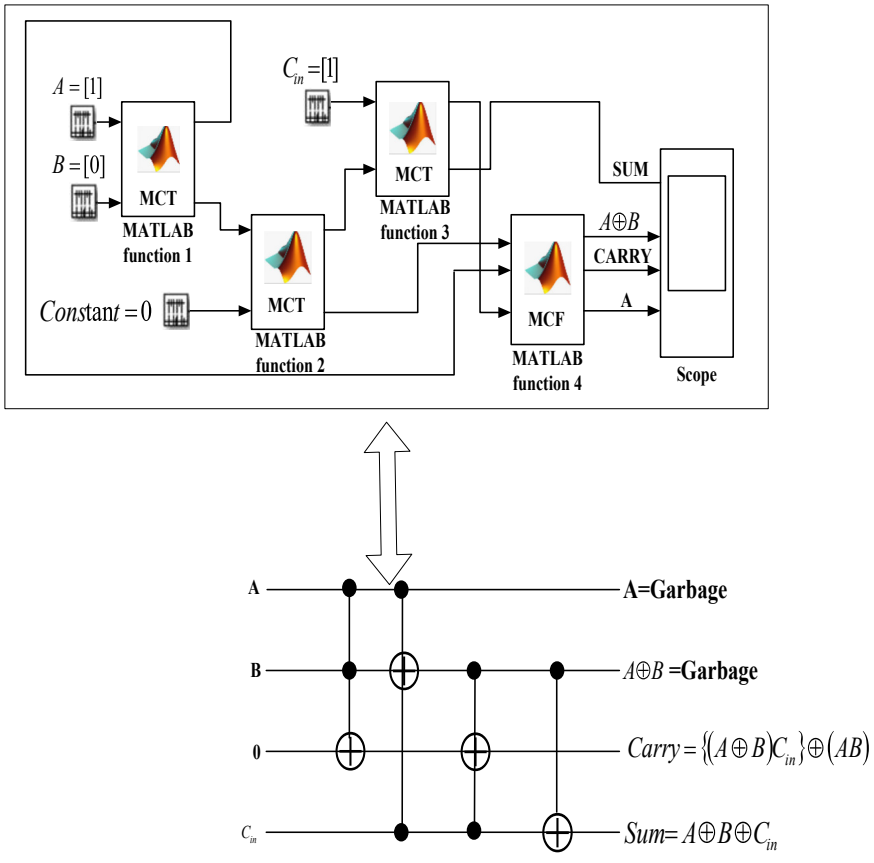

Fig. 1. Reversible Full Adder design utilizing Multiple Control Toffoli gate and Multiple Control Fredrick gate

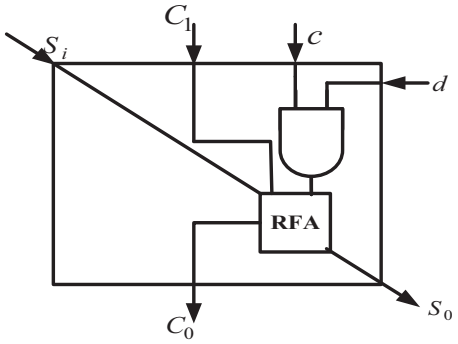

Fig. 3. Baugh-Wooley Multiplier white-cell

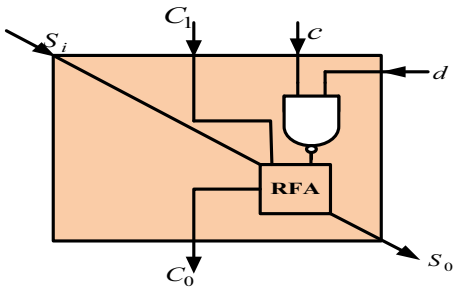

Fig. 4. Baugh-Wooley Multiplier pink-cell

(diagonal-black line), carry output (vertical black line). Each cell has 4 inputs with 2 outputs, the reversible amplifier cell is constructed into a cell with 5 inputs as well as 5 outputs to maintain reversible multiplier cell. Among these, 3 outputs have remained as garbage outputs. These are defined as don't care outputs, because it may be left not mentioned, it leads to incomplete mentioned process.

They create 2 outputs: sum output (diagonal-black line), carry output (vertical black line).

This is performed based on the following example: Let the counts be multiplied by A and B. Wherein A implies $m-bit$ multiplier, B implies $m-bit$ multiplicand, A multiplier and B multiplicand are used to perform the signed $m\times m$ multiplication without variation when the results have similar bit-width as inputs. For example: $-2\ ^{*}\ 3$ is -6, its binary representation $(0010)_2 \times (0011)_2 = (1010)_2$. What occurs if the outcome is in "$2m$" bits. Either needs to utilize sign extension or $2m\times 2m$ array multiplier. Baugh-Wooley multiplication is a proficient approach to deal in such situations.

The Baugh-Wooley has been developed for 2's-complement count. Consider two $m-$ bit numbers, C and D to be multiplied. C and D are expressed in given equation (3 and 4),

$$C = -c_{m-1}2^{m-1} + \sum_{j=0}^{m-2} c_j 2^j \tag{3}$$

$$D = -d_{m-1}2^{m-1} + \sum_{i=0}^{m-2} d_i 2^i \tag{4}$$

here c_j and d_i are represented as bits in C and D respectively, c_{m-1} and d_{m-1} are represented as sign bits. The product is expressed in given equation (5 and 6),

$$P = C\times D \tag{5}$$

$$P = c_{m-1}d_{m-1}2^{2m-2} + \sum_{j=0}^{m-2}\sum_{i=0}^{m-2} c_j d_i 2^{j+i} - 2^{m-1}\sum_{j=0}^{m-2} c_j d_{m-1}2^j - 2^{m-1}\sum_{i=0}^{m-2} c_{m-1}d_i 2^i \tag{6}$$

The above equation indicates that the final product is obtained by subtract the last 2 positive terms from the first 2 terms.

Assume C and D are 4-bit binary numbers, then the product $P = C\times D$ is 8-bits long and is given in equation (7),

$$P = c_3 d_3 2^6 + \sum_{j=0}^{2}\sum_{i=0}^{2} c_j d_i 2^{j+i} + 2^3\sum_{j=0}^{2}\overline{d_3 c_j}2^j + 2^3\sum_{i=0}^{2}\overline{c_3 d_i}2^i - 2^7 + 2^4 \tag{7}$$

Equation (7) is known as design of Baugh-Wooly Multiplier utilizing Reversible Full Adder with multiple control Toffoli and Fredrick gate. With the help of this algorithm, Baugh-Wooley Multiplier reduces delay, power consumption and the area.

4. RESULTS AND DISCUSSION

This section describes the Baugh-Wooley Multiplier design using Multiple Control Toffoli and Multiple Control Fredrick gate Reversible Logic gates. The simulation of proposed BWM-MCT-MCF multiplier design is done in MATLAB, PC along Intel Core i5, 2.50 GHz CPU, 8 GB RAM, Windows 7. The performance of the proposed BWM-MCT-MCF design is analyzed under certain performance metrics. The obtained results are compared with existing designs, such as BWM-FG-FRG, BWM-TG-FG, BWM-RL-TG.

4.1. Performance metrics

The performance of the proposed BWM-MCT-MCF design is analyzed with performance metrics, like constant inputs, garbage outputs, gate count, quantum cost.

4.1.1. Gate count and hardware complex. An important factor during design evaluation is to scale the reversible logic depending on the count of gates. It helps to find out the hardware complexity. But the proposed circuit proves that hardware complexity is better than existing approaches, because any logic (AND, OR, EXOR, NOR gates) in the design can be implemented within minute. So, the hardware complexity of the Baugh-Wooley Multiplier design is decreased.

4.1.2. Constant inputs. Garbage/constant input is the input that is utilized as control input through coupling either logical lower or higher for obtaining the desired operation in the output. The count of constant inputs is a key consideration of reversible logic circuit designing.

4.1.3. Garbage outputs. It indicates the count of reversible gate outputs that are not performing beneficial functions. Optimizing garbage output is another restriction on reversible logic circuit design.

Table 1 shows the performance analysis of the performance metrics. Here, Power, Delay, quantum cost are analyzed for determining the proposed BWM-MCT-MCF performance. The proposed approach attains 23.94%, 21.94%, 24.94% lower gate count; 25.75%, 16.86%, 33.86% lower constant input; 23.88%, 27.87%, 21.54% lower Garbage outputs; 15.88%, 21.65%, 32.54% lower Power consumption; 26.87%, 25.55%, 26.97% lower Delay; 26.87%, 21.33%, 20.66% lower Quantum cost are compared with the existing designs, such as BWM-FG-FRG, BWM-TG-FG, and BWM-RL-TG, respectively.

5. FPGA IMPLEMENTATION OF PROPOSED BAUGH WOOLEY MULTIPLIER

In this section, the implementation of the proposed BWM-MCT-MCF is discussed. Then the designed BWM-MCT-MCF is implemented using the Xilinx ISE tool with the Virtex 5 device along Intel (R) Core (TM) 2 Duo CPU T6600 @ 3.2 GHz, system. FPE320 is a 3U VPX FPGA processor board in Xilinx Virtex-5 FPGAs available with an FMC mezzanine site. The performance metrics, such as power and delay are analyzed. The reversible multiplier architectures are designed and implemented using the Xilinx ISE tool to calculate the delay. Xpower analysis tool is used to calculate the power. Then the performance of the proposed FPGA-BWM-MCT-MCF method is compared with the existing designs, like FPGA-BWM-RL-TG [20], FPGA-BWM-TG-FG [21].

Table 1. Performance analysis

Performance metrics	BWM-FG-FRG	BWM-TG-FG	BWM-RL-TG	BWM-MCT-MCF (Proposed)
Gate count	44	42	40	16
Constant inputs	52	44	42	12
Garbage outputs	52	50	49	28
Quantum cost	37	32	28	18

Figure 5 shows the FPGA implementation of Baugh-Wooley Multiplier in Vertex 5 kit. Figure 6 displays the RTL Schematic of BWM. Figure 7 depicts the Simulation Result of BWM. Figure 8 portrays the Device utilization of BWM.

5.1. Performance analysis

The performance metrics, like power consumption, number of input LUTs, number of occupied slices, voltage, current and delay are analyzed.

Table 2 displays the performance analysis of the power consumption, number of input LUTs, number of occupied slices, voltage, current and delay for determining the proposed FPGA-BWM-MCT-MCF performance. Then the performance of the proposed method provides 15.88%, 21.65%, lower power consumption; 23.84%, 28.04% lower number of LUTs, 43.83%, 28.83%, number of occupied slices, equal voltage, 24.93%, 27.923% lower current consumption 26.87%, 25.55%, lower delay compared with the existing designs, such as FPGA-BWM-TG-FG, FPGA-BWM-RL-TG respectively.

Fig. 5. FPGA implementation of Baugh-Wooley Multiplier in Vertex 5 kit

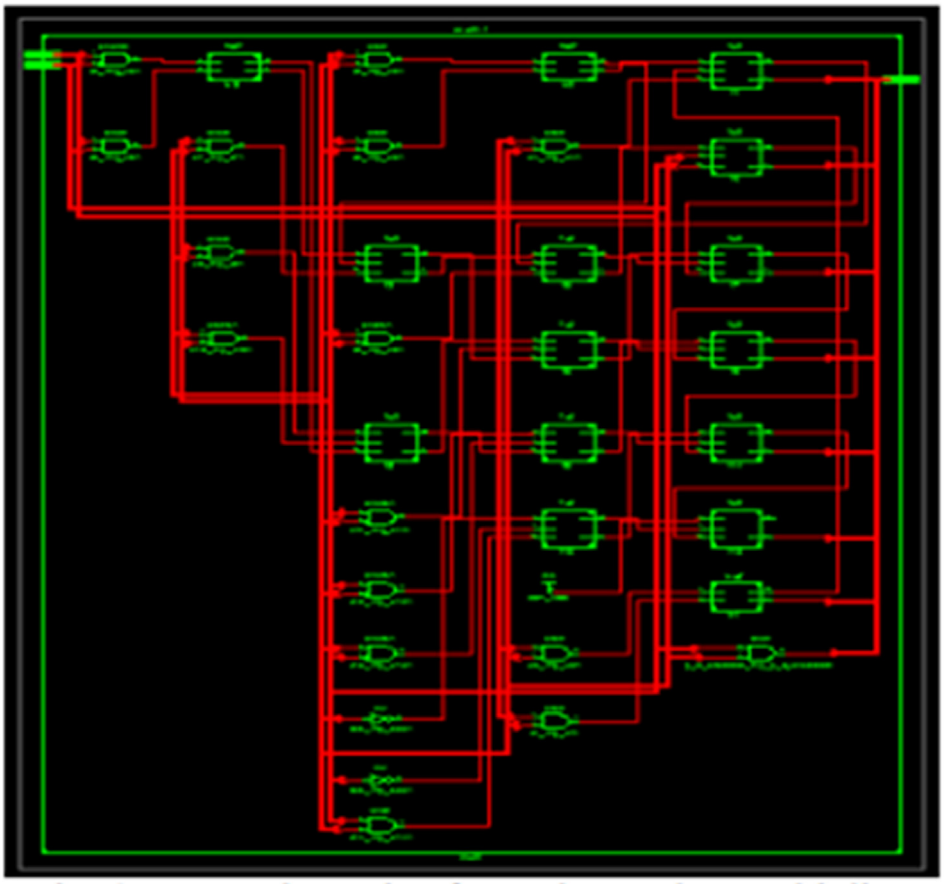

Fig. 6. RTL schematic of Baugh-Wooley Multiplier

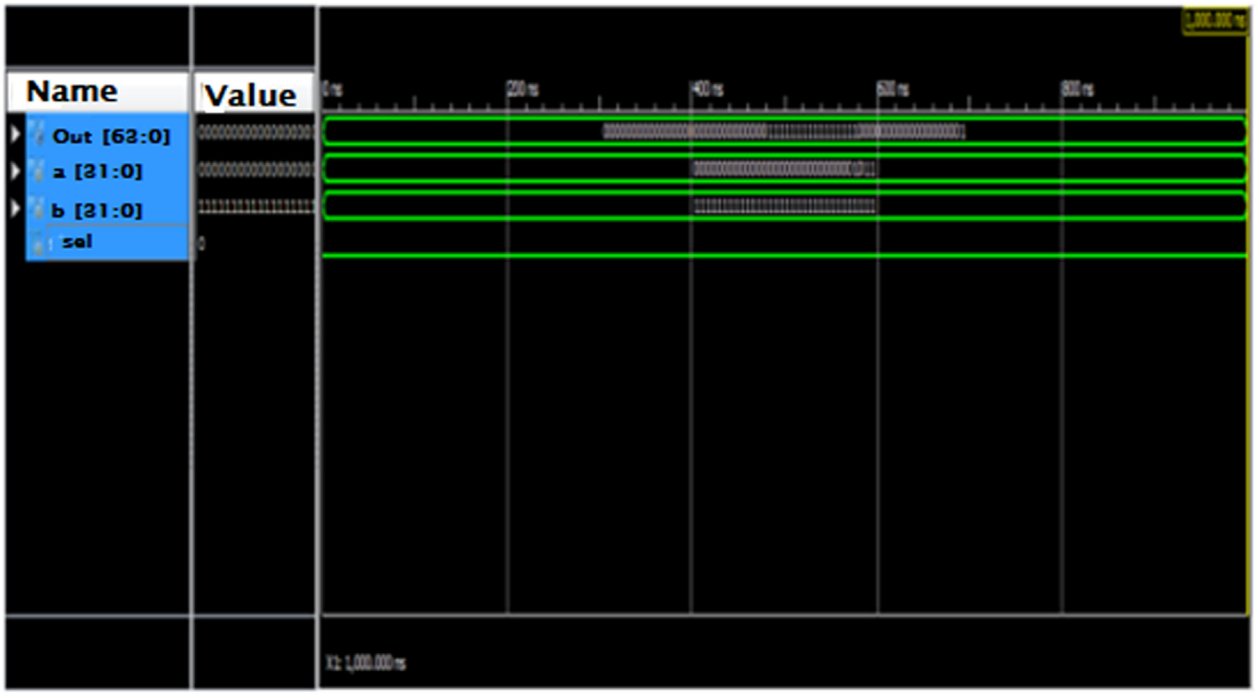

Fig. 7. Simulation result of Baugh-Wooley Multiplier

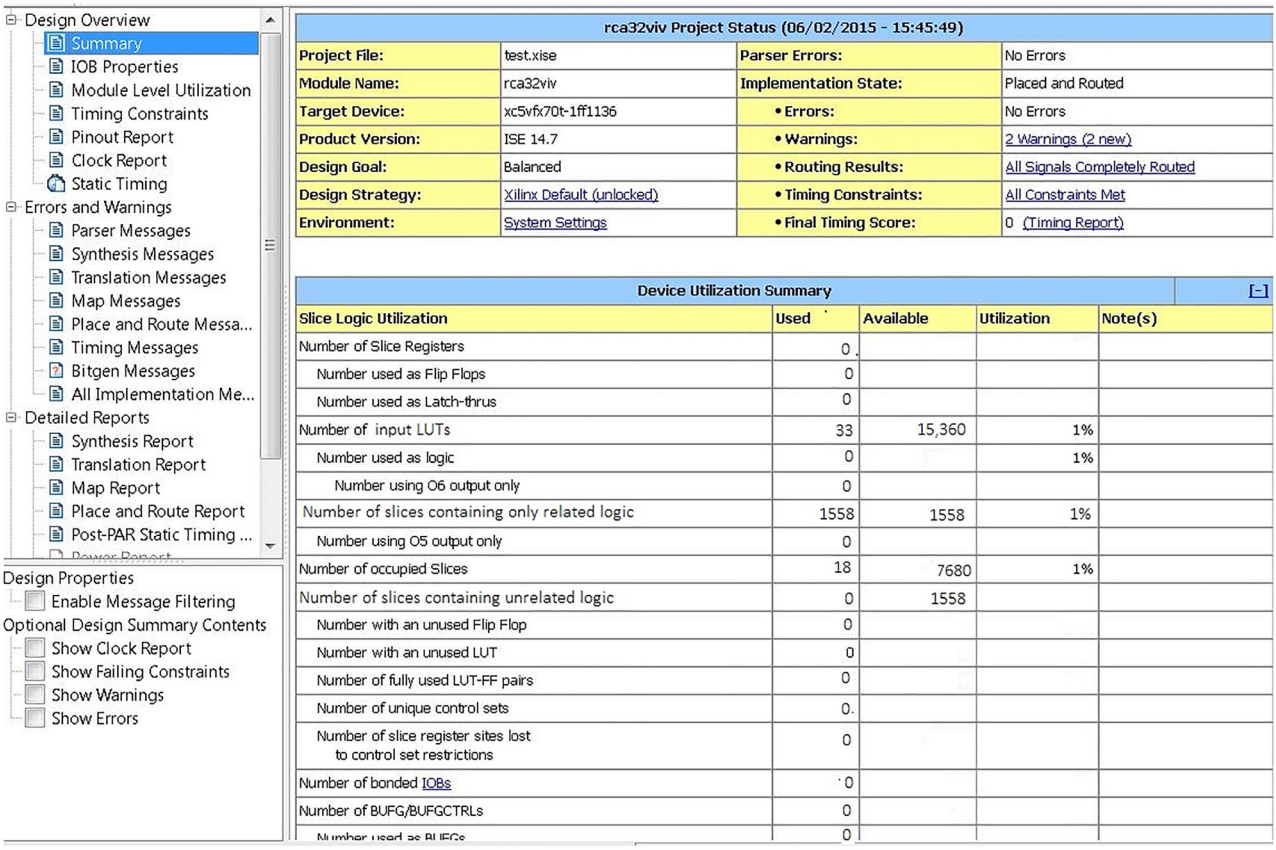

Fig. 8. Device utilization of Baugh-Wooley Multiplier

Table 2. Performance Analysis of delay and power

Performance metrics	Methods		
	FPGA-BWM-TG-FG	FPGA-BWM-RL-TG	FPGA-BWM-MCT-MCF (Proposed)
Number of input LUTs	79	57	33
Number of occupied slices	77	53	18
Voltage	0.76W	0.76W	0.076W
Current Consumption	0.45A	0.65A	0.26A
Delay	178.34	169.03	89.10
Power consumption	729.33	684.45	515.12

6. CONCLUSION

The Baugh-Wooley Multiplier is successfully designed in this manuscript using Multiple Control Toffoli (MCT) and Multiple Control Fredrick gate (MCF) Reversible Logic gates. The proposed BWM-MCT-MCF multiplier is done in MATLAB. Finally, the proposed BWM-MCT-MCF method attains lower quantum cost 23.86%, 25.87%, 31.63% compared with the existing designs, like BWM-FG-FRG, BWM-RL-TG, BWM-TG-FG respectively. Then the designed BWM-MCT-MCF is implemented using the Xilinx ISE tool with the Virtex 5 device. Here, the proposed FPGA-BWM-MCT-MCF method attains lower power 32.75%, 15.86% compared with the existing designs, like FPGA-BWM-RL-TG, FPGA-BWM-TG-FG, respectively.

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