AKADÉMIAI KIADÓ

UNIVERSITY of DEBRECEN

International Review of Applied Sciences and Engineering

14 (2023) 1, 100–113

DOI:
10.1556/1848.2022.00448

ORIGINAL RESEARCH PAPER

An assessment of advanced DC-link based reversing voltage type multilevel inverter topologies

S. Nagaraja Rao[1*], B.M. Manjunatha[2], A. Suresh Kumar[2], B.M. Kiran Kumar[1], R. Satish Kumar[2] and S. Pranupa[1]

[1] Department of Electrical Engineering, M S Ramaiah University of Applied Sciences, Bangalore, India

[2] Department of Electrical and Electronics Engineering, Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal, Andhra Pradesh, India

Received: December 31, 2021 • Accepted: October 6, 2022
Published online: December 7, 2022

ABSTRACT

In this paper, advanced DC-Link (DCL) based reversing voltage type Multilevel Inverter (MLI) topologies by compensating the difficulties in the conventional MLIs are reviewed. These topologies consist of less switching components and driver circuits when compared with conventional MLIs predominantly in higher levels. Consequently, installation area, total cost and hardware difficulties are reduced by increasing the voltage levels. The unipolar based Pulse Width Modulation Schemes (PWMS) will improve DCL inverters performance. This paper presents unipolar Multi-Reference (MR) based sine and space vector PWMS with single triangular carrier wave for generating required levels in output voltage. Comparison between UMR sine and space vector PWMS for DCL inverter topologies is presented in terms of Fundamental Output Voltage (FOV) and Total Harmonic Distortion (THD). The research tries to establish the survey analysis for single-phase 7-level DCL based reversing voltage type MLI topologies with UMR based sine and space vector PWMs. Finally, to confirm the feasibility of proposed DCL-MLIs in terms of FOV and THD the simulation results are incorporated. Further, the prototype model is developed for single-phase 7-level DCL inverter with Field Programmable Gate Array (FPGA) based UMR sine and space vector PWMS to authenticate simulation results. The efficiency of the proposed cascaded MLI achieves the value of 99.003%.

KEYWORDS

diode clamped-DCL, capacitor clamped-DCL, cascaded-DCL, sine PWMS, space vector PWMS, THD

1. INTRODUCTION

The increase in electrical energy demand leads to depletion in conventional sources. It also leads to widespread research on power generation using renewable sources as solar and wind energy. The power output of these energy converters highly depends on environmental conditions; it results in wide research scope in the field of power system and power electronics. This leads to development of new converter topologies with required operation, power management, and control. The most necessary circuit in Renewable Energy applications is inverter; it converts generated DC into AC and it is fed to load or grid. The conventional Multi-Level Inverters (MLIs) were used during earlier days [1]. These MLIs continue to have more consideration due to high voltage, low device stress, less switching losses, high efficiency and less THD. The conventional MLIs primarily classified Diode clamped MLI (DCMLI) [2], Flying capacitor MLI (FCMLI) [3] and cascaded MLI (CMLI) [4]. These MLIs use high switching components, capacitors, and clamping diodes. As the number of levels 'm' increases power switches vary accordingly i.e., conventional MLIs

*Corresponding author.
E-mail: nagarajarao.ee.et@msruas.ac.in

require '2 × (m–1)' but the DCL based MLIs require '(m+3)'. A review on Conventional MLIs with respect to their applications was disclosed in [5–13]. The output of conventional MLIs contains harmonics, so bulky and expensive filters must be used before loading or powering the application stage. The application and number of levels on output with conventional MLI is limited due to high voltage stress, switching loss and complex control.

To overcome the limitation with conventional inverter, numerous topologies are introduced by the researchers in [14–17]. The key research view is to design the MLIs with reduced components for producing output voltage with more levels. These MLIs receive more attention due to high voltage operation capability, improved power quality, output with near sine waveform, reduced number of switching components, high efficiency, and reduced switching losses, less complex and low electromagnetic interference. These proposed topologies will operate with single or multiple sources. If it is operating with single source, capacitors are used as potential dividers or if it operates with multi sources, it may be with equal or unequal magnitude. If it is unequal, it may be with ratios such as 1:2:3… or 1:2:4… Also all the switches used in the circuit will operate at same frequency or with different frequencies.

With the advances in MLI topologies, challenges raise in controlling the switches with appropriate Pulse Width Modulation (PWM) schemes [18–21]. The considerable advance in PWM methods has been observed over the years. The PWM methods are classified as low or fundamental switching and high switching PWM methods. The low switching frequency PWM provides considerable performance when compared with high frequency PWM techniques [14]. Also, PWM methods are classified as Sinusoidal PWM (SPWM) and SVPWM, these approaches will have high switching frequency and provide faster transient response [15, 16]. The topology with boost control is proposed in [18], this topology has reduced number of switches, operates with single source with capacitors as potential dividers. The voltage balancing across potential dividers is obtained with simple technique. Furthermore, based on the carrier based PWM systems it was categorized as Phase Shifted PWM (PSPWM) [21] and Level Shifted PWM (LSPWM) method [19, 20]. In LSPWM technique [22] the carriers used may be either unipolar or bipolar and based on how the carrier is distributed it is classified as Phase Dispose PWM (PDPWM), Phase Opposition Dispose PWM (PODPWM) as well as Alternate Phase Opposition Dispose PWM (APODPWM).

Currently, there has been a substantial growth of interest in multilevel energy conversion. However, the currently utilized inverter topologies are mostly discussed as useable multi-level inverters. A few methods of the above mentioned topologies are called 3/2 cascade multilevel inverter (CMLI) [23, 24]. Certain uses for novel converters have industrial drives [25], flexible AC transmission systems (FACTS) [26], as well as vehicle propulsion [27]. The efficiency and power quality are of great concern to investigators [28].

Certain novel methods have recently been presented like topology using high-power, low-switching-frequency devices [29]. Though the topology consists of certain modifications to decrease output, the overall drawback of this system contains low-order current harmonics [30]. In [31], the multilevel output is created using multi-winding transformer.

This paper presented a review on advanced DCL based MLI topologies based on a single-phase 7-level DCL. It consists of Full-bridge inverter (FBI) and DCL. The DCL can be capacitor clamped or diode clamped or cascaded, used to obtain required positive or negative steps and FBI is used to change the polarity. When compared to the conventional MLIs, the DCL based MLI topologies can have enriched performance by employing the UMR based PWMS [32]. This paper presents the UMR with Space Vector PWMS to increase FOV and reduce THD [33] for DCL based MLIs and compare the performance of the Space Vector based PWMS with sinusoidal PWMS.

The most utilized topologies are fixed neutral point [34], the floating capacitor [35] and cascaded H-bridge inverter [36]. Most of them are controlled by sinusoidal PWM extended to multicarrier arrays of two sorts: level shifted (LS-PWM) called phased array, and phase shifted (PS-PWM) [37]. The modulation approaches have multilevel extension of SVM [38], multilevel selective harmonic removal [39], and multilevel space vector control [40]. These modulation systems are theoretically conceived as an inverter powered by a constant DC link. At real applications, the capacitor voltage has considerable ripple [41]. Ripple becomes significant when non-linear loads are powered. This low frequency ripple is transmitted to load based on low pass nature of load. This low-frequency cannot be modified under open loop uses, it could be somewhat remunerated for by drivers on closed loop [42].

2. STRUCTURE OF DCL BASED REVERSING VOLTAGE TYPE MLI

The block diagram of DCL based reversing voltage type MLI is shown in Fig. 1 [43]. The main idea with reversing voltage type MLI is that the level generating circuit produces positive stepped waveform and the full-bridge circuit generates negative as well as positive levels in output voltages.

At conventional multilevel inverters, semiconductor switches combine to create high-frequency waveforms. However, it is not necessary to use all the switches to produce bipolar levels. One portion is named level generation

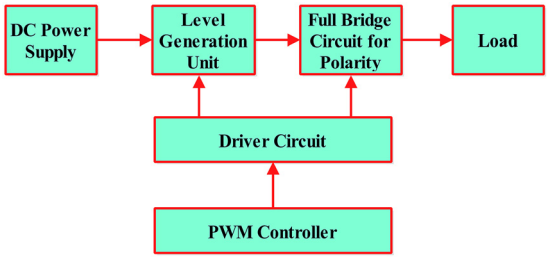


Fig. 1. Block diagram of DCL based reversing voltage type MLI

part on positive polarity. The topology merges two portions (high and low frequency). The seven level RV topology is presented in Fig. 1. In Figure 1, level generation unit creates the necessary output levels with positive polarities of output voltage and reversing the direction of voltage is obtained by using full bridge circuit.

This topology is simply extended to greater voltage levels by doubling the intermediate phase presented in Fig. 1. This topology utilizes isolated DC supplies. So there are no face voltage balance problems based on fixed DC voltage values. Compared to cascade topology, it needs only one third (1/3) of the isolated power supplies utilized at cascade-type inverter.

Figure 1 can be extended to three-phase inverter for seven levels using delta-connected three-phase load. The DCL based reversing voltage type multilevel topology is fed to full bridge converter to produce necessary voltage levels. The secondary transformer is delta connected (Δ) related to three-phase system. Another benefit of this topology is the need of half as many conventional carriers. Thus, implementing multilevel inverter use decreased the count of carriers. Another drawback of this topology is that the entire switches must be chosen among fast switches.

There is no need to use all high frequency switches in DCL based reversing voltage type MLI topologies. This topology divides the circuit into two parts, which are the polarity and level producing circuits. The level generation circuit generation levels with positive polarity, and polarity circuit generates the positive and negative levels on output voltage. The level generation circuit requires maximum frequency power switchers and the polarity reversing circuit requires slow frequency power switches that work at fundamental frequency.

3. PROBLEM FORMULATION – DCL BASED REVERSING VOLTAGE TYPE MLI TOPOLOGIES

3.1. Diode clamped-DCL (DC-DCL) inverter

Figure 2 shows the three-phase 7-level DC-DCL inverter based on diode clamped phase-leg and FBI.

Table 1 gives comparison details of conventional and DCL based MLI for obtaining 7-level output for diode clamped type MLI. It clearly shows a considerable reduction of the number of components with the suggested structure [44, 45]. The percentage reduction in components will be high with increase in the number of levels as mentioned before. Table 2 presents switching states of DC-DCL inverter to generate required output phase voltages.

3.2. Capacitor clamped-DCL (CC-DCL) inverter

Figure 3 presents the arrangement of single-phase 7-level CC-DCL inverter depending on capacitor clamped phase-leg and FBI. Table 3 shows comparison details of conventional and DCL based MLI for obtaining7-level output for capacitor clamped type MLI.

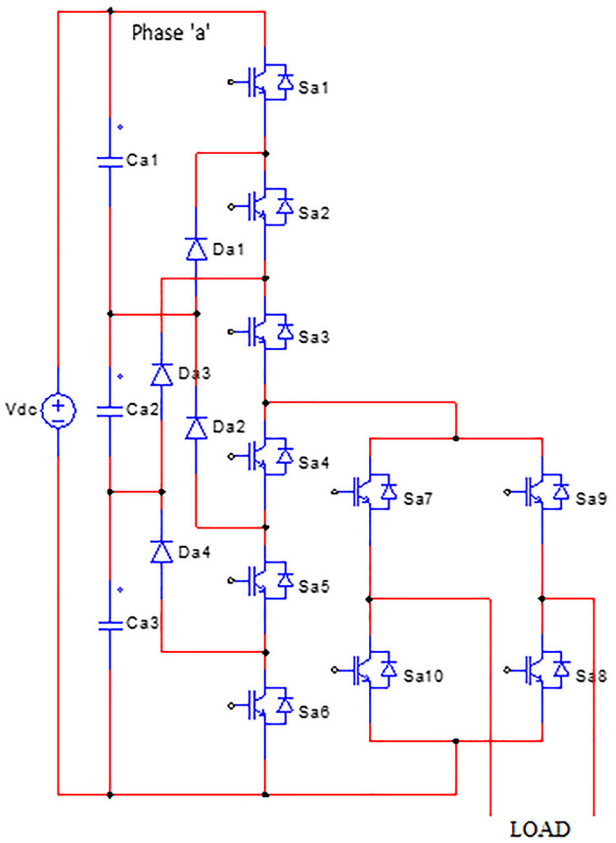


Fig. 2. DC-DCL based reversing voltage type inverter

Table 1. Components comparison of conventional and DCL inverter for diode clamped MLIs

Components	Diode clamped type	
	Conventional	DCL
Switches	12	10
Clamping diodes	10	4
Voltage splitting capacitors	6	3

Table 2. Switching states of DC-DCL inverter

S. No	Conduction paths for the DC-DCL based reversing voltage type inverter	Voltage levels
1	$C_{a3} - C_{a2} - C_{a1} - S_{a1} - S_{a2} - S_{a3} - S_{a7} -$ Load $- S_{a8}$	$+3V_{dc}$
2	$C_{a3} - C_{a2} - S_{a2} - S_{a3} - S_{a4} - S_{a7} -$ Load $- S_{a8}$	$+2V_{dc}$
3	$C_{a3} - S_{a3} - S_{a4} - S_{a5} - S_{a7} -$ Load $- S_{a8}$	$+V_{dc}$
4	$S_{a4} - S_{a5} - S_{a6} - S_{a7} -$ Load $- S_{a8}$	0
5	$C_{a3} - S_{a3} - S_{a4} - S_{a5} - S_{a9} -$ Load $- S_{a10}$	$-V_{dc}$
6	$C_{a3} - C_{a2} - S_{a2} - S_{a3} - S_{a4} - S_{a9} -$ Load $- S_{a10}$	$-2V_{dc}$
7	$C_{a3} - C_{a2} - C_{a1} - S_{a1} - S_{a2} - S_{a3} - S_{a9} -$ Load $- S_{a10}$	$-3V_{dc}$

Table 4 presents the switching states of CC-DCL inverter to generate required output phase voltages.

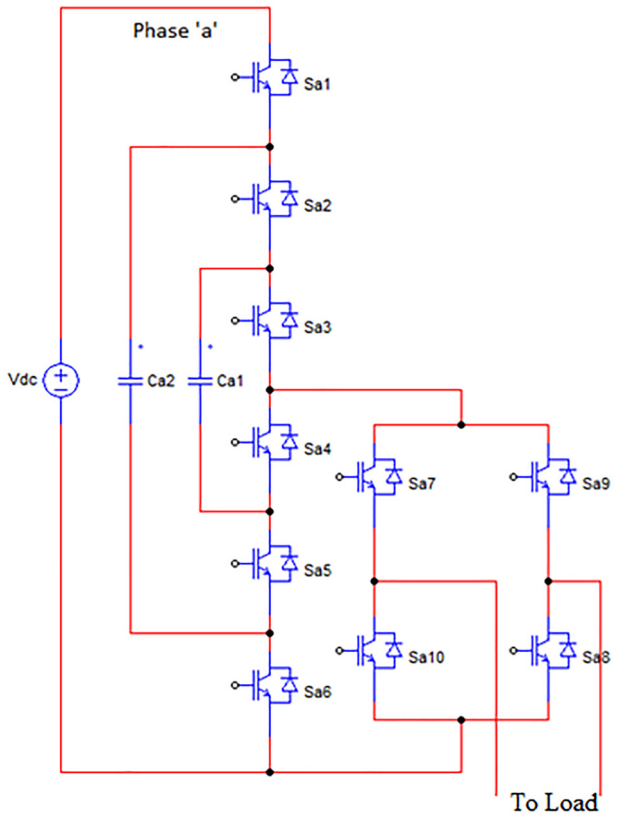


Fig. 3. CC-DCL based reversing voltage type inverter

Table 3. Components comparison of conventional and DCL inverter for capacitor clamped type MLIs

Components	Capacitor clamped type	
	Conventional	DCL
Switches	12	10
Clamping Capacitors	5	2

Table 4. Switching states of CC-DCL inverter

S. No	Conduction paths for the CC-DCL based reversing voltage type inverter	Voltage levels
1	$V_{dc} - S_{a1} - S_{a2} - S_{a3} - S_{a7} - Load - S_{a8}$	$+3V_{dc}$
2	$C_{a1} - S_{a1} - S_{a2} - S_{a4} - S_{a7} - Load - S_{a8}$	$+2V_{dc}$
3	$C_{a2} - S_{a1} - S_{a5} - S_{a4} - S_{a7} - Load - S_{a8}$	$+V_{dc}$
4	$S_{a4} - S_{a5} - S_{a6} - S_{a7} - Load - S_{a8}$	0
5	$C_{a2} - S_{a1} - S_{a5} - S_{a4} - S_{a9} - Load - S_{a10}$	$-V_{dc}$
6	$C_{a1} - S_{a1} - S_{a2} - S_{a4} - S_{a9} - Load - S_{a10}$	$-2V_{dc}$
7	$V_{dc} - S_{a1} - S_{a2} - S_{a3} - S_{a9} - Load - S_{a10}$	$-3V_{dc}$

3.3. Cascaded-DCL (C-DCL) inverter

Figure 4 shows the single-phase 7-level C-DCL inverter [46, 47]. Each cascade unit is created by relating half-bridge cells in series. Table 5 gives comparison details of conventional and DCL based MLI for obtaining 7-level output for cascaded type MLI. It clearly shows that there is a considerable reduction of the number of components with the suggested structure [5, 48]. The percentage reduction in components will be high through the number of levels as mentioned before. Table 6 presents switching states of C-DCL inverter to generate essential output phase voltages.

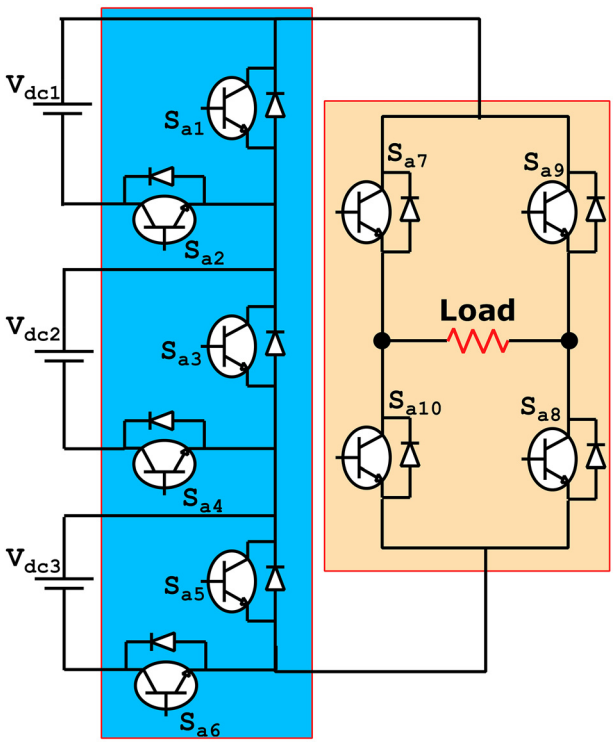


Fig. 4. C-DCL based reversing voltage type inverter

Table 5. Components comparison of conventional and C-DCL inverter for cascaded type MLIs

Components	Cascaded type	
	Conventional	C-DCL
Switches	12	10
DC	3	3
Clamping diodes	0	0
Capacitors	0	0

Table 6. Switching states of C-DCL inverter

S. No	Conduction paths for the C-DCL based reversing voltage type inverter	Voltage levels
1	$S_{a6} - V_{dc3} - S_{a4} - V_{dc2} - S_{a2} - V_{dc1} - S_{a7} - Load - S_{a8}$	$+3V_{dc}$
2	$S_{a5} - S_{a4} - V_{dc2} - S_{a2} - V_{dc1} - S_{a7} - Load - S_{a8}$	$+2V_{dc}$
3	$S_{a5} - S_{a3} - S_{a2} - V_{dc1} - S_{a7} - Load - S_{a8}$	$+V_{dc}$
4	$S_{a5} - S_{a3} - S_{a1} - S_{a7} - Load - S_{a8}$	0
5	$S_{a5} - S_{a3} - S_{a2} - V_{dc1} - S_{a9} - Load - S_{a10}$	$-V_{dc}$
6	$S_{a5} - S_{a4} - V_{dc2} - S_{a2} - V_{dc1} - S_{a9} - Load - S_{a10}$	$-2V_{dc}$
7	$S_{a6} - V_{dc3} - S_{a4} - V_{dc2} - S_{a2} - V_{dc1} - S_{a9} - Load - S_{a10}$	$-3V_{dc}$

At this configuration, the magnitude of all DC voltage sources is maintained at similar value (Vdc1 = Vdc2 = Vdc3).

The peak output voltage will be the sum of the entire input of DC voltages, whose magnitude is provided in Eq. (1).

$$V_{o,\max} = \sum_{i=1}^{S} V_{\mathrm{dci}} V_{o,\max} = \sum_{i=1}^{S} V_{\mathrm{dci}} \tag{1}$$

Therefore, C-DCL MLI topology, to generate 7-level output requires 3 DC and 1 H-bridge circuit. Equation (1) represents output level of reversing voltage type MLI. By using the polarity generation unit, both negative and positive levels are obtained in the output. The synthesized voltage levels in the output will be obtained using Eqs (2) and (3).

$$V_0,\ \max = \sum_{i=1}^{n} + V_i,\ \text{If } S_{a7}, S_{a8} = 1 \tag{2}$$

$$V_0,\ \max = \sum_{i=1}^{n} - V_i,\ \text{If } S_{a9}, S_{a10} = 1 \tag{3}$$

The estimated C-DCL based reversing voltage type MLI output voltage levels are given in Eq. (4).

$$N_{\mathrm{Levels},1} = (2S + 1)^H \tag{4}$$

where '*S*' refers to the number of DC sources.

The power switches for C-DCL based MLI can be estimated by using Equation (5).

$$N_S = 2\ (S_1 + S_2 + \ldots\ldots S_n) + 4\ H \tag{5}$$

The generalized output wave form of the 7-level DCL based reversing voltage type MLI is presented in Fig. 5.

This topology splits the output voltage into two portions. One portion is known as level generation part at positive polarity. This portion requires maximum frequency switches to produce the essential levels. The other portion is known as polarity generation part and it is in charge of producing the polarity of output voltage. The topology syndicates two portions (high and low frequency) to yield the multilevel voltage output. The seven-level RV topology is shown in Fig. 4. The key idea of C-DCL based MLI topology is left side of the circuit produces essential output voltage levels. This portion is called as level generation unit, whereas, full bridge inverter is essential to change the positive polarity of voltage to a negative polarity.

This topology is simply extended to maximum voltage levels by doubling intermediate phase and is shown in Fig. 4. The maximum voltage levels including intermediate phase are shown in Fig. 4. Consequently, there are no voltage balance issues based on fixed DC voltage values. Based on

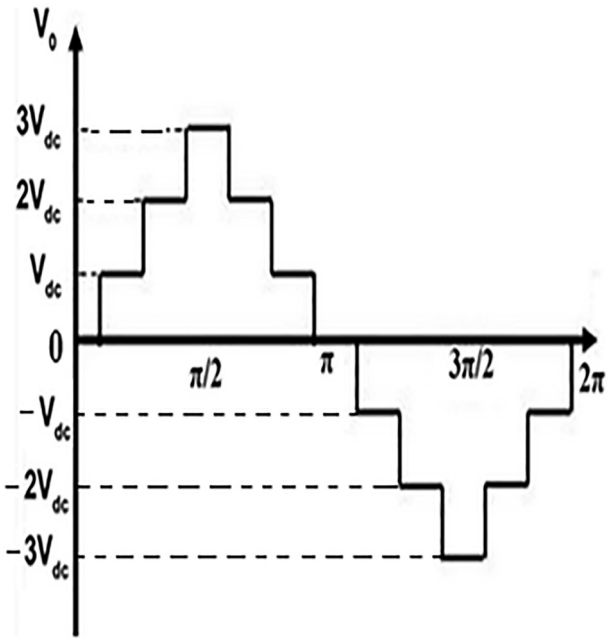


Fig. 5. Estimated 7-level output

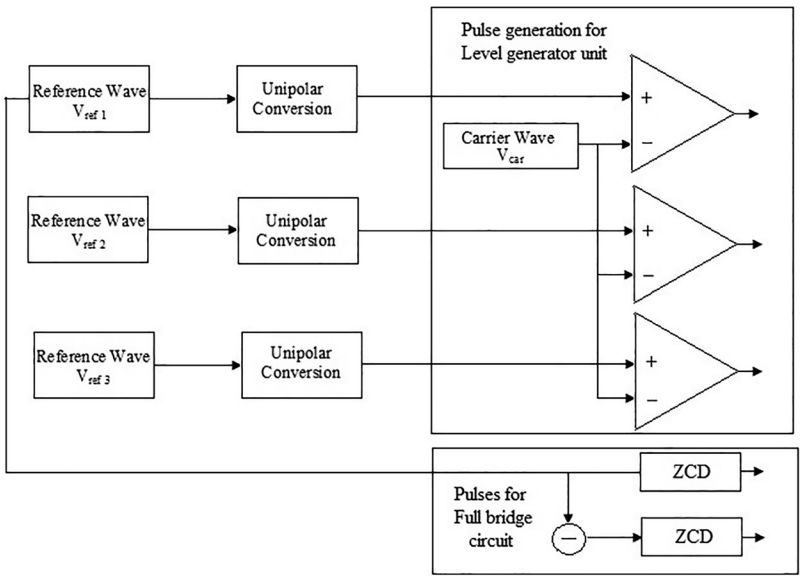


Fig. 6. Pulses generation for 7-level DCL based MLIs

Fig. 4, the multilevel positive voltage is based on full-bridge converter. The secondary transformer is delta connected (Δ) to a 3-phase system. This topology needs fewer components compared to conventional inverters. The multilevel converter operates only on positive polarity and does not create negative polarities. Thus, it executes multilevel inverter through decreased number of carriers. Another drawback of this topology is that the all the switches must be chosen from among fast switches.

4. MODULATION STRATEGIES

In this paper, unipolar MR based PWMS is incorporated with sine and modified space vector references to generate pulses for DCL inverters. These reference signals are sampled at each carrier cycle by triangular carrier signal, as the modulation is symmetric. The carrier signal is triangular waveform train using 'fc' frequency and 'Ac' amplitude [49, 50]. The methods for producing pulses is depicted in Fig. 6 for the DCL based MLIs for 7-level.

For 'm' levels, (m-1/2) references are required for obtaining pulses for RV inverters. i.e, for 7-level inverters three reference signals (V_{ref1}, V_{ref2} and V_{ref3}) are used for carrier signal ($V_{carrier}$). This theoretical modulation index (M) with single carrier and multiple reference is defined as

$$M = \frac{A_m}{\frac{(m-1)}{2} * A_c} \tag{6}$$

The 'M' for DCL based MLIs for 7-level is defined as

$$M = \frac{A_m}{3 * A_c} \tag{7}$$

For illustrating PWMS for DCL based reversing voltage type MLIs, a 7-level inverter with $M = 0.8$ and $m_f = 10$ are shown in Fig. 7(a) and (b), for the MR base sine and modified space vector modulation signals respectively.

Pulses are required for H-Bridge to obtain positive and negative levels on output voltage. The pulse generator is set with amplitude '1' and operating with fundamental frequency of 50Hz. The switches S_{a7} and S_{a8} are triggered at the same instant with zero degree delay with pulse generator as well as power switches S_{a9} and S_{a10} are triggered with the delay of 180° with pulse generator. If switches S_{a7} and S_{a8} are turned ON, the positive levels will be obtained across the load, while operation of switches S_{a9} and S_{a10} causes negative levels to appear across the load.

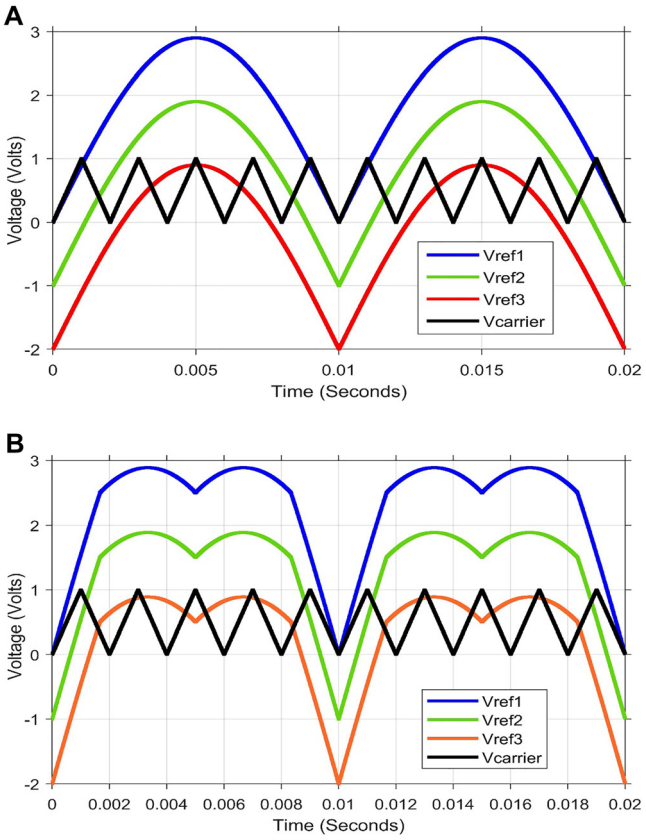


Fig. 7. a) Multi-Reference Sinusoidal PWM (MRSPWM) with triangular carrier; b) Multi-Reference SVPWM (MRSVPWM) with triangular carrier

5. COMPARISON WITH CONVENTIONAL MLIS

This section presents the comparison of DC-Link based reversing voltage type MLI topologies with conventional MLIs based on the number of levels generated for a given components count.

5.1. Comparison of switching devices and number of levels

The number of components essential in a host of inverter topologies to obtain a definite level of output are presented in Table 7 to bring out the importance of reversing voltage

Table 7. Component count comparison

Topologies/Components	Diode clamped type		Capacitor clamped type		Cascaded type	
	Conventional	DCL	Conventional	DCL	Conventional	DCL
Main Switches	2 (m–1)	m+3	2 (m–1)	m+3	2 (m–1)	m+3
Main Diodes	2 (m–1)	m+3	2 (m–1)	m+3	2 (m–1)	m+3
Clamping diodes	2 (m–3)	(m–3)	0	0	0	0
Balancing capacitors	0	0	(m–2)	(m–3)/2	0	0
DC bus capacitors	m–1	(m–1)/2	0	0	0	0

type MLI topologies. However, as the number of output level increases, the main switches are maximized by '2 (m–1)' and 'm+3' correspondingly for conventional and advanced DCL based reversing voltage type MLI topologies.

Figure 8 presents graphical representation for comparison of essential number of switching components among conventional and advanced DCL MLI topologies. This study revealed that the diode clamped based MLIs have more clamping diodes, absence of modularity, and unbalanced voltages. In capacitor clamped based MLIs, more clamping capacitors are required, along with charge unbalancing of capacitors at minimum switching frequency and voltage balance control being the main issues. The only disadvantage of cascaded based MLI is that it needs a greater number of separate dc sources. It can be decided that C-DCL based reversing voltage type MLI has superior advantages over diode clamped and capacitor clamped MLI topologies.

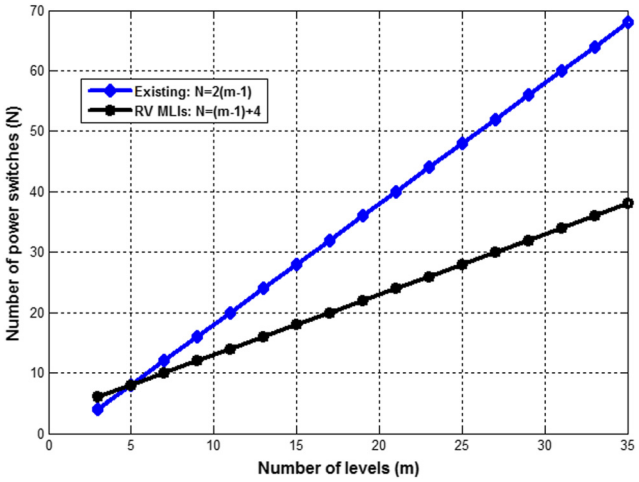


Fig. 8. Comparison of required number of switches

5.2. Comparison of components count, weight and cost

The components count, weight and cost ($) comparison has been analyzed for the DC-Link based reversing voltage type and conventional MLIs, capacitor clamped and cascaded inverters. The switch IGBT – FD300R06KE3, Capacitor – C4DEFP-Q6380A8TK and Diodes – 85HF60 are considered for all MLIs to have a precise comparison. Table 8 shows the required components, weight and cost comparison of all the inverters. Figures 9 and 10 give the weight and cost comparison. From Figs 9 and 10, it is clear that the C-DCL inverter has less weight and cost when compared to other inverters.

Table 8. Comparison of MLIs in terms of components count, weight and cost to generate7-levels

Topologies/Components	Diode clamped type		Capacitor clamped type		Cascaded type	
	Conventional	DCL	Conventional	DCL	Conventional	DCL
Main switches	12	10	12	10	12	10
Clamping diodes	8	4	0	0	0	0
Clamping capacitors	0	0	5	2	0	0
DC bus capacitors	6	3	0	0	0	0
DC sources	1	1	1	1	3	3
Weight	7.149 kg	5.11 kg	6.594 kg	5.03 kg	5.337 kg	4.657 kg
Cost in $	134,830	98,092	122,244	92,228	102,102	88,442

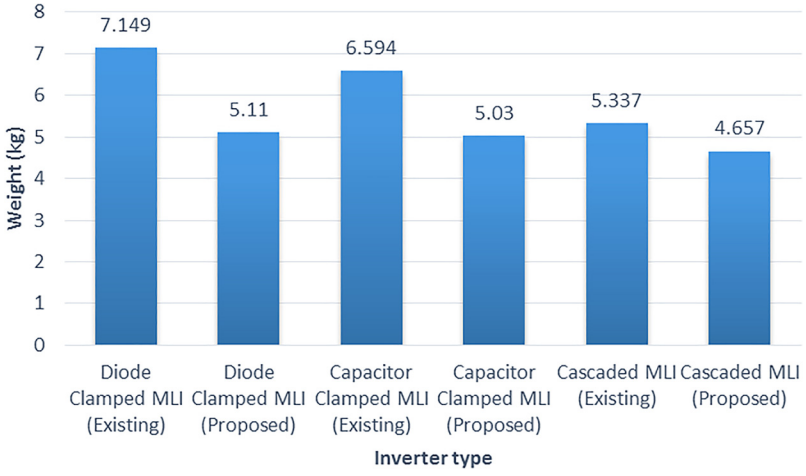


Fig. 9. Comparison of MLIs in terms of weight

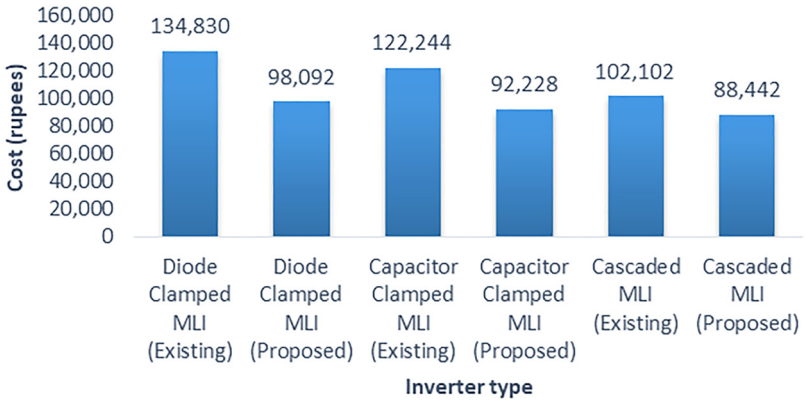


Fig. 10. Comparison of MLIs in terms of cost ($)

6. SIMULATION RESULTS

To check the performance of DC-Link based reversing voltage type MLIs the detailed simulation was carried out using multiple reference SPWM and multiple reference SVPWM strategies with a single triangular carrier. During assessment of DC-MLI, CC-MLI and C-MLI fed R-Load are analyzed with 400 V input voltage, 5 KHz frequency and 10Ω load with variation of '*M*' from 0.3 to 0.8.

6.1. DC-DCL based reversing voltage type MLI

The simulated AC output of 1–Φ 7-level DC-DCL inverter with MRSPWM and MRSVPWM single carrier and its FFT analysis are shown in Figs 11 and 12 for $M = 0.8$.

Figure 11(a) depicts the simulated waveform of 7-level DC-DCL inverter output with MRSPWM. The FOV of DC-DCL inverter is 237.9 V. Figure 11(b) represents the THD of the DC-DCL inverter. The DC-DCL inverter is 24.19%.

Figure 12(a) portrays simulation results of DC-DCL inverter output with MRSVPWM. The FOV of DC-DCL inverter is 273.8 V. Figure 12(b) signifies THD of DC-DCL inverter. The %THD of DC-DCL inverter is 21.68%. When compared to the MRSPWM technique %THD value decreases; in-addition, this topology was replicated and investigated for different modulations. The simulation results along with THD are presented in Table 9.

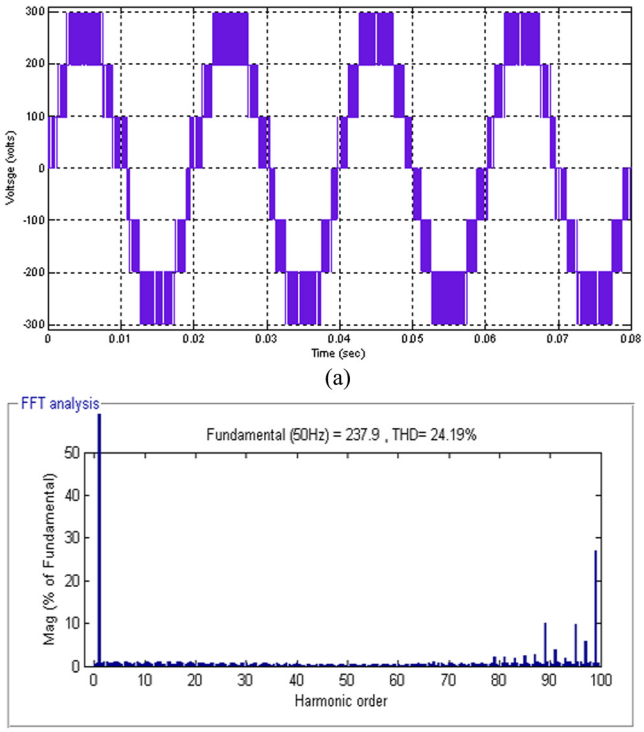


Fig. 11. DC-DCL inverter with MRSPWM (a) Phase Voltage (b) THD analysis

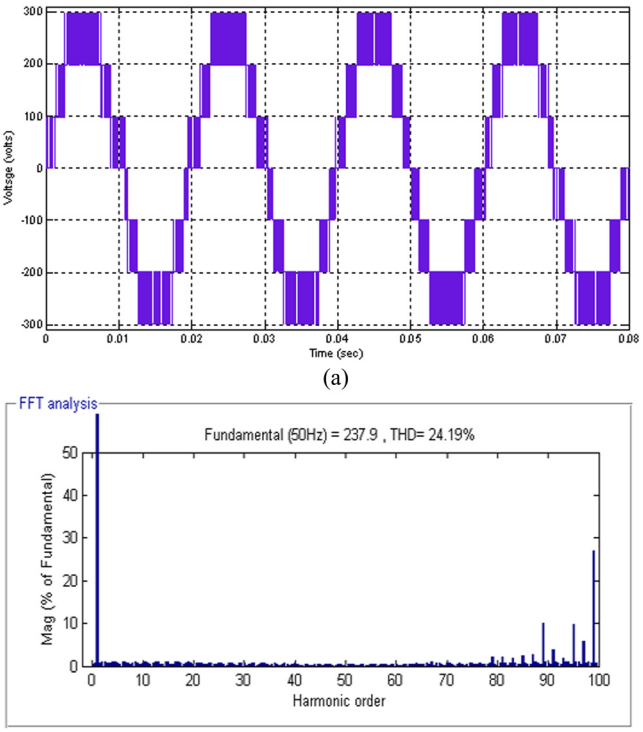


Fig. 12. DC-DCL inverter with MRSVPWM (a) Phase Voltage (b) THD analysis

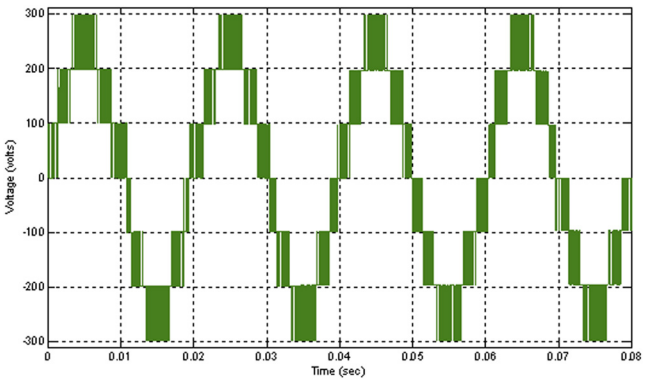
Table 9. FOV (V_{rms}) and % THD for various PWM techniques for DC-DCL inverter

Modulation index (M)	Number of levels	PWM technique			
		MRSPWM		MRSVPWM	
		V_{rms}	% THD	V_{rms}	% THD
0.8	7- Level	168.2	24.19	193.6	21.68
0.7	7- Level	147	25.02	169.3	24.15
0.6	5- Level	126	33.19	144.9	25.35
0.5	5- Level	104.9	39.99	120.7	35.26
0.4	5- Level	83.83	44.14	96.46	41.86
0.3	3- Level	62.86	63.88	72.27	48.92

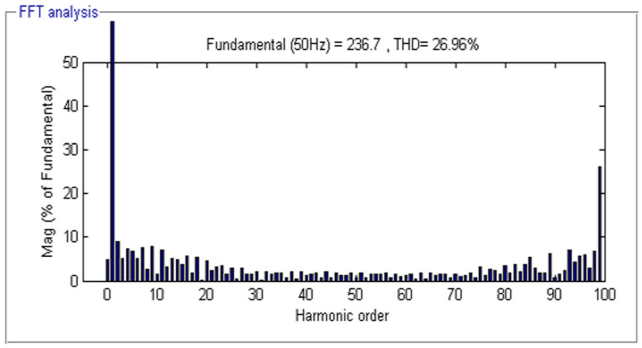
6.2. CC-DCL based reversing voltage type inverter

The simulated AC output of 1–Φ 7-level CC-DCL with MRSPWM and MRSVPWM using single carrier and its FFT analysis are shown in Figs 13–14 for $M = 0.8$. Figure 13(a) represents the simulation results of the 7-level CC-DCL based reversing voltage type inverter output with MRSPWM. The FOV is 236.7 V. Figure 13(b) represents the THD of CC-DCL inverter. The %THD of CC-DCL inverter is 26.96%.

Figure 14(a) represents the simulation results of 7-level CC-DCL inverter output using MRSVPWM. The FOV is 272.6 V. Figure 14(b) shows the THD of CC-DCL inverter. The %THD value of CC-DCL inverter is 24.48%. When compared to the MRSPWM technique %THD value decreases. This topology was simulated and analyzed with different modulation indices. The simulation results along with THD are presented in Table 10.

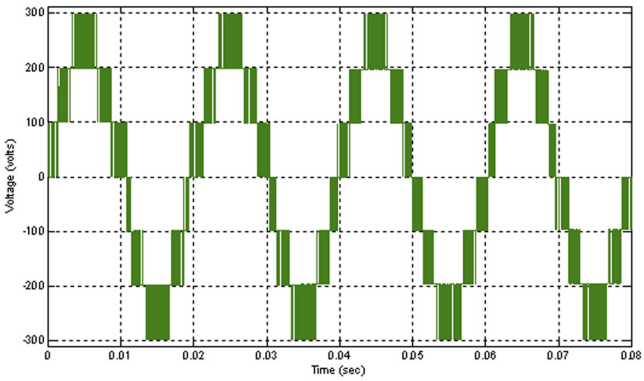


(a)

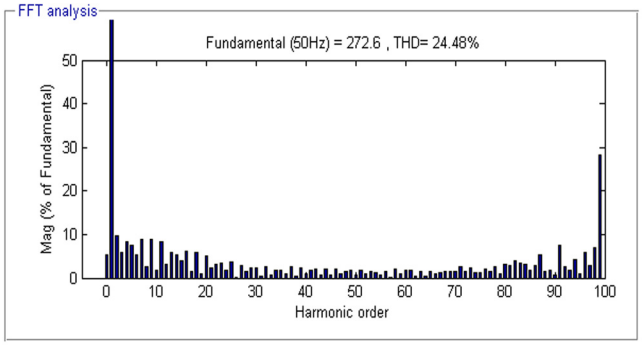


(b)

Fig. 13. CC-DCL inverter with MRSPWM (a) Phase voltage (b) THD analysis



(a)



(b)

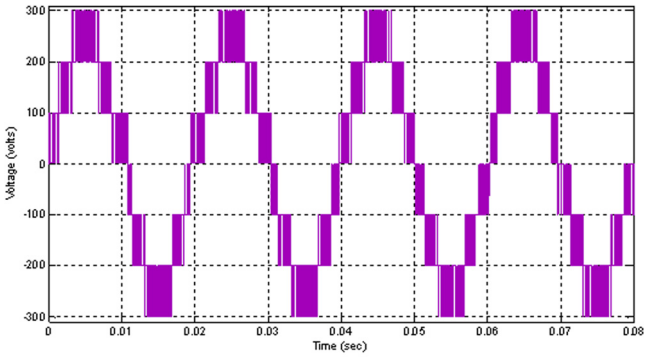
Fig. 14. CC-DCL inverter with MRSVPWM (a) Phase voltage (b) THD analysis

6.3. C-DCL based reversing voltage type inverter

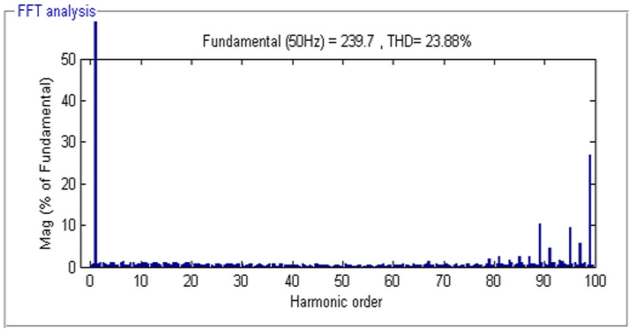
The simulated AC output voltage of the 1–Φ 7-level C-DCL inverter with MRSPWM and MRSVPWM with single triangular carrier and its FFT analysis are shown in Figs 15 and 16 for $M = 0.8$. Figure 15(a) represents the simulation voltage waveform of 7-level C-DCL inverter with MRSPWM. The FOV is 239.7 V. Figure 15(b) shows the THD of C-DCL inverter. The %THD value of C-DCL

Table 10. FOV (V_{rms}) and % THD for various PWM techniques for CC-DCL inverters

Modulation index (M)	Number of levels	PWM technique			
		MRSPWM		MRSVPWM	
		V_{rms}	% THD	V_{rms}	% THD
0.8	7- Level	167.4	26.96	192.8	24.48
0.7	7- Level	145.9	27.77	168.8	26.91
0.6	5- Level	125.6	35.47	144.2	27.99
0.5	5- Level	104.5	41.91	120	37.56
0.4	5- Level	83.2	46.24	96.01	44.04
0.3	3-Level	62.05	66.11	71.78	50.65

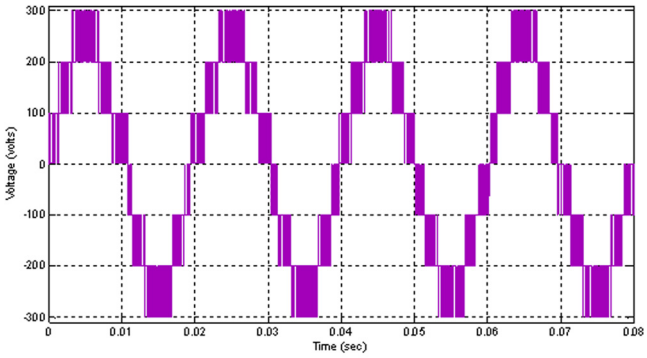


(a)

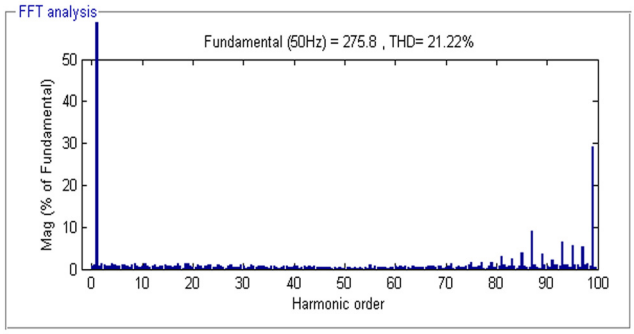


(b)

Fig. 15. C-DCL inverter with MRSPWM (a) Phase voltage (b) THD analysis



(a)



(b)

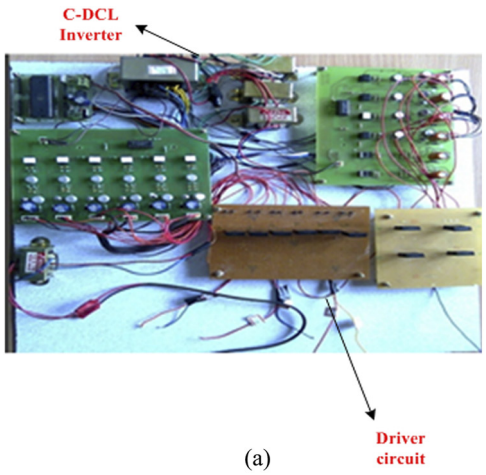
Fig. 16. C-DCL inverter with MRSVPWM (a) Phase voltage (b) THD analysis

inverter implies 23.88%. Figure 16(a) represents the simulation voltage waveform of 7-level C-DCL inverter with MRSVPWM. The FOV is 275.8 V. Figure 16(b) shows the THD of C-DCL inverter. The %THD value of C-DCL inverter is 21.22%. When compared to the MRSPWM technique %THD value decreases. This topology was simulated and analyzed with different modulation indices. The simulation results along with THD are presented in Table 11.

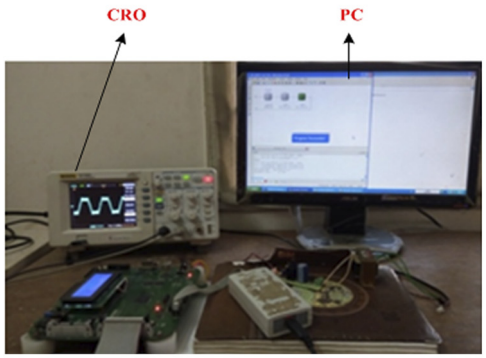
From Tables 9–11 it is concluded that C-DCL inverter using MRSVPWM scheme with a single triangular carrier

Table 11. FOV (V_{rms}) and % THD for various PWM techniques for 1–Φ7-level C-DCL inverters

Modulation index (M)	Number of levels	PWM technique			
		MRSPWM		MRSVPWM	
		V_{rms}	% THD	V_{rms}	% THD
0.8	7- Level	169.6	23.89	195	21.34
0.7	7- Level	148.6	24.47	170.7	23.80
0.6	5- Level	127	33.28	146.1	24.91
0.5	5- Level	106	39.39	122	34.66
0.4	5- Level	84.85	43.55	97.54	41.08
0.3	3- Level	63.5	63.5	73.14	48.03



(a)



(b)

Fig. 17. 7-level C-DCL inverter (a) Prototype model (b) VHDL program implementation in FPGA

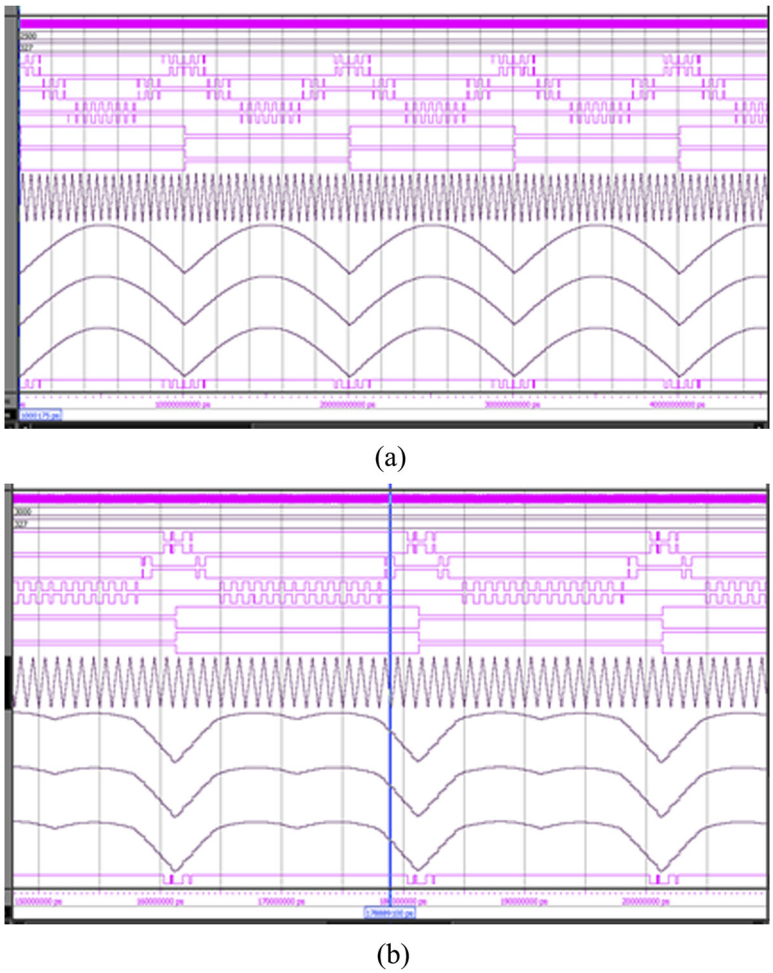


Fig. 18. Pulse generation through Xilinx ISE (a) using MRSPWM (b) using MRSVPWM

has given good THD with FOV when compared with MRSPWM technique.

7. HARDWARE IMPLEMENTATION OF C-DCL INVERTER

The prototype model of the C-DCL based reversing voltage type MLI is carried out for 7-level with Xilinx Spartan FPGA to authenticate the simulation outcomes [46, 47]. The C-DCL inverter is fed with R-load during hardware implementation and it is depicted in Fig. 17(a) and (b). It consists of PC, Buffer circuit, Opto isolator, FPGA controller, Driver circuit, and C-DCL inverter.

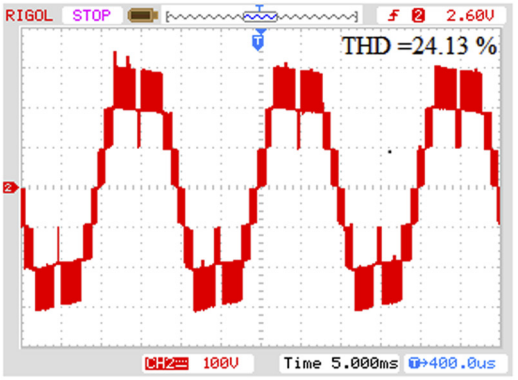
Generation of gate pulses with MRSPWM and MRSVPWM systems using Xilinx ISE is presented in Fig. 18 (a) and (b), respectively.

The FOV is 193.6 V and %THD of C-DCL inverter is 22.16%. Tables 11 and 12 present experimental and simulation outcomes with phase voltage and THD of C-DCL inverter. From the experimental and simulation outcomes of phase voltage and THD of DC-DCL, CC-DCL and C-DCL based reversing voltage type MLI topologies with MR based PWMS it can be seen that maximal FOV and reduced THD is obtained with MRSVPWM scheme. From the THD analysis it is perceived that THD in output voltage of 1-ϕ 7-level C-DCL inverter using MRSPWM and MRSVPWM modulation methods is 23.89% and 21.34%, respectively, for 'M' of 0.8.

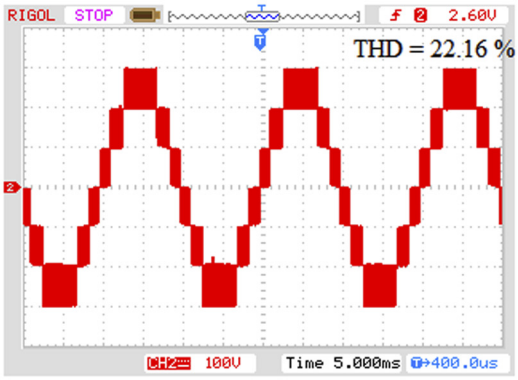
%THD of experimental system is measured using digital oscilloscope and THD results are presented in Fig. 19 (a)

Table 12. Experimental comparison of FOV (V_{rms}) and THD for 7-level ($m = 7$)

		PWM schemes with triangular carrier			
		MRSPWM		MRSVPWM	
Modulation index (M)	Number of levels	V_{rms}	% THD	V_{rms}	% THD
0.8	7- Level	167.8	24.13	193.6	22.16
0.7	7- Level	146.3	25.68	168.2	24.57
0.6	5- Level	125.1	34.84	143.6	26.02
0.5	5- Level	103.83	41.23	120.86	36.32
0.4	5- Level	81.52	45.36	95.26	43.12
0.3	3- Level	61.02	65.26	71.58	49.92



(a)



(b)

Fig. 19. Phase voltages of C-DCL inverter for $M = 0.8$ and $M_f = 100$ (a) Using MRSPWM (b) Using MRSVPWM

and (b) for MRSPWM and MRSVPWM methods, respectively. It is perceived that, harmonic in output voltages is 24.13% and 22.16% respectively with '*M*' of 0.8. Thus, the simulation results of the C-DCL inverter for 7-level are interpreted with respect to the experimental results with an acceptable error of 2%. The results analysis reveals that the FOV and THD values are varied inversely with different modulation indices.

Table 13 explains the efficiency of conventional and proposed topology. The proposed topology affirms the best result over the conventional topology. The efficiency values of the proposed topology are 99.003%.

Table 14 shows the DC-link balancing and voltage deviation.

Table 13. Efficiency for various topologies

Various topologies	Efficiency obtained (%)
Cascaded MLI (Proposed)	99.003
Cascaded MLI (Existing)	80.343
Capacitor clamped MLI (Proposed)	75.603
Capacitor clamped MLI (Existing)	55.893
Diode clamped MLI (Proposed)	79.6432
Diode clamped MLI (Existing)	61.0093

Table 14. Framing of DC link balancing and voltage deviation

DC link balancing		Voltage deviation	
Cascaded MLI (Existing)	Cascaded MLI (Proposed)	Cascaded MLI (Existing)	Cascaded MLI (Proposed)
0.28230	0.01093	10	4.5
0.04717	0.01095	11	5

8. CONCLUSIONS

An assessmet of 7-level DCL based DC-MLI, CC-MLI and C-MLI topologies was carried out with respect to power switches, weight, cost, driver circuits, FOV and %THD. When compared to other well-known and recent MLI topologies, DCL-based MLI topologies have fewer power switches, carrier signals require less installation space. The DCL based reversing voltage type MLIs are utilized in domestic/industrial uses like Back-to-Back converters. The presented advanced DC-DCL, CC-DCL and C-DCL based reversing voltage type MLI topologies will increase the efficiency, decreasing the size and cost of prototype related to conventional MLIs. The switches and gate drivers are selected and tested with the ready to print PCB designs and simulations, to implement them in the hardware for all the discussed circuits of inverters in future research work.

ACKNOWLEDGMENT

The authors would like to express their gratitude to VC and RUAS management, who provided the vital facilities for this investigation study.

REFERENCES

[1] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of modulation and control techniques for multilevel inverters in traction applications," *IEEE Access*, vol. 9, pp. 24187–204, 2021.

[2] K.K. Gupta, A. Ranjan, P. Bhatnagar, L.K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Trans. Power Electronics*, vol. 31, no. 1, pp. 135–51, 2015.

[3] H. P. Vemuganti, S. Dharmavarapu, S. K. Ganjikunta, H. M. Suryawanshi, and H. A. Rub, "A survey on reduced switch count multilevel inverters," *IEEE Open J. Ind. Electronics Soc.*, 2021.

[4] A. Bughneda, M. Salem, A. Richelli, D. Ishak, and S. Alatai, "Review of multilevel inverters for PV energy system applications," *Energies*, vol. 14, no. 6, p. 1585, 2021.

[5] C. Dhanamjayulu, and S. Meikandasivam, "Implementation and comparison of symmetric and asymmetric multilevel inverters for dynamic loads," *IEEE Access*, vol. 6, pp. 738–46, 2017.

[6] J. S. M. Ali, R. S. Alishah, N. Sandeep, S. H. Hosseini, E. Babaei, K. Vijayakumar, and U. R. Yaragatti, "A new generalized multilevel converter topology based on cascaded connection of basic units,"

IEEE J. Emerging Selected Top. Power Electronics, vol. 7, no. 4, pp. 2498–512, 2018.

[7] J. S. M. Ali, R. S. Alishah, and V. Krishnasamy, "A new generalized multilevel converter topology with reduced voltage on switches, power losses, and components," *IEEE J. Emerging Selected Top. Power Electronics*, vol. 7, no. 2, pp. 1094–106, 2018.

[8] N. R. Sulake, A. K. DevarasettyVenkata, and S. B. Choppavarapu, "FPGA implementation of a three-level boost converter-fed seven-level dc-link cascade H-bridge inverter for photovoltaic applications," *Electronics*, vol. 7, no. 11, p. 282, 2018.

[9] P. Rajesh, S. Muthubalaji, S. Srinivasan, and F.H. Shajin, "Leveraging a dynamic differential annealed optimization and recalling enhanced recurrent neural network for maximum power point tracking in wind energy conversion system," *Technol. Econ. Smart Grids Sustain. Energy*, vol. 7, no. 1, pp. 1–5, 2022.

[10] F.H. Shajin, P. Rajesh, and M.R. Raja, "An efficient VLSI architecture for fast motion estimation exploiting zero motion prejudgment technique and a new quadrant-based search algorithm in HEVC," *Circuits, Systems, Signal. Process.*, vol. 41, no. 3, pp. 1751–74, 2022.

[11] P. Rajesh, F.H. Shajin, B. Rajani, and D. Sharma, "An optimal hybrid control scheme to achieve power quality enhancement in micro grid connected system," *Int. J. Numer. Model. Electron. Networks, Devices Fields*, 2022, Paper no. e3019.

[12] F.H. Shajin, and P. Rajesh, "FPGA realization of a reversible data hiding scheme for 5G MIMO-OFDM system by chaotic key generation-based paillier cryptography along with LDPC and its side channel estimation using machine learning technique," *J. Circuits, Syst. Comput.*, vol. 31, no. 5, 2022, Paper no. 2250093.

[13] S. Pranupa, A. T. Sriram, and S. N. Rao, "Wind energy conversion system using perturb & observe-based maximum power point approach interfaced with T-type three-level inverter connected to grid," *Clean Energy*, August 2022, vol. 6, no. 4, pp. 534–49. https://doi.org/10.1093/ce/zkac034.

[14] H. Samsami, A. Taheri, and R. Samanbakhsh, "New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures," *IET Power Electronics*, vol. 10, no. 11, pp. 1315–23, 2017.

[15] B. M. Manjunatha, S. N. Rao, A. S. Kumar, K. S. Zabeen, S. Lakshminarayanan, and A. V. Reddy, "An optimized multilevel inverter topology with symmetrical and asymmetrical DC sources for sustainable energy applications. Engineering," *Technol. Appl. Sci. Res.*, vol. 10, no. 3, pp. 5719–23, 2020.

[16] M. Jayabalan, B. Jeevarathinam, and T. Sandirasegarane, "Reduced switch count pulse width modulated multilevel inverter," *IET Power Electronics*, vol. 10, no. 1, pp. 10–7, 2017.

[17] E. J. Lee, and K. B. Lee, "Performance improvement of cascaded H-bridge multilevel inverters with modified modulation scheme," *J. Power Electronics*, vol. 21, no. 3, pp. 541–52, 2021.

[18] S. N. Rao, D. V. Kumar, and C. S. Babu, "Implementation of multilevel boost DC-link cascade based reversing voltage inverter for low THD operation," *J. Electr. Eng. Technol.*, vol. 13, no. 4, pp. 1528–38, 2018.

[19] E. Babaei, and S. Laali, "Optimum structures of proposed new cascaded multilevel inverter with reduced number of components," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6887–95, 2015.

[20] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimization assessment of a new extended multilevel converter topology," *IEEE Trans. Ind. Electronics*, vol. 64, no. 6, pp. 4530–8, 2017.

[21] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-Type) module: asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electronics*, vol. 63, no. 11, pp. 7148–56, 2016.

[22] V. K., M. B. Matam, and A. K. D. Venkata, Mallapu, "Evaluation of impedance network based 7-level switched capacitor multi level inverter for single phase grid integrated system," *J. Inst. Eng. (India) Ser. B*, vol. 99, no. 6, pp. 623–33, 2018.

[23] T. L. Skvarenina, *The Power Electronics Handbook*. Boca Raton, FL, CRC Press, 2002.

[24] X. Yun, Y. Zou, X. Liu, and Y. He, "A novel composite cascade multilevel converter," *Proc. 33rd IEEE IECON*, 2007, pp. 1799–804.

[25] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conf. Rec. 34th IEEE IAS Annu. Meeting*, Vol. 4, 1999, pp. 2662–9.

[26] E. Najafi, and A. H. M. Yatim, "A novel current mode controller for a static compensator utilizing Goertzel algorithm to mitigate voltage sags," *Energy Convers. Manage.*, vol. 52, no. 4, pp. 1999–2008, 2011.

[27] K. Nakata, K. Nakamura, S. Ito, and K. Jinbo, "A three-level traction inverter with IGBTs for EMU," *Conf. Rec. IEEE IAS Annu. Meeting*, Vol. 1, 1994, pp. 667–72.

[28] K. Y. Lau, M. F. M. Yousof, S. N. M. Arshad, M. Anwari, and A. H. M. Yatim, "Performance analysis of hybrid photovoltaic/diesel energy system under Malaysian conditions," *J. Energy*, vol. 35, no. 8, pp. 3245–55, 2010.

[29] G. M. Martins, J. A. Pomilio, S. Buso, and G. Spiazzi, "Three-phase low frequency commutation inverter for renewable energy systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1522–8, 2006.

[30] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–12, 2008.

[31] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P. N. Enjeti, "Multilevel inverter by cascading industrial VSI," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 832–8, 2002.

[32] B. M. K. Kumar, S. N. Rao, and M. S. Indira, "Analysis of grid-connected reduced switch MLI with high-gain interleaved boost converter and hybrid MPPT for solar PV," *Int. J. Energy Environ. Eng.*, vol. 13, pp. 1287–307, 2022. https://doi.org/10.1007/s40095-022-00479-4.

[33] M. Hegde, S. N. Rao, and M. S. Indira, "Modified cascaded reversing voltage multilevel inverter using optimal switching angle technique for photovoltaic applications," *Innovations in Electrical and Electronic Engineering*, 2021, pp. 319–38.

[34] A. Nabae, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. 17, no. 5, pp. 518–23, 1981.

[35] T. Meynard, and H. Foch, "Multi-level choppers for high voltage applications," *Eur. Power Electron. J.*, vol. 2, no. 1, pp. 45–50, 1992.

[36] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non conventional power converter for plasma stabilization," *Proc. Power Electronics Specialist Conf.*, 1988, pp. 122–9.

[37] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, 1992.

[38] N. Celanovic, and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–41, 2001.

[39] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters," *Proc. Industry Appl. Annu. Meet.*, pp. 1454–61, 1998.

[40] J. Rodríguez, L. Morán, P. Correa, and C. Silva, "A vector control technique for medium-voltage inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 882–8, 2002.

[41] J. Rodríguez, P. Lezana, J. Pontt, J. Espinoza, and M. Pérez, "Input current harmonics in a regenerative multi-cell inverter with single-phase active rectifiers," *Proc. Industrial Electronics Society Annu. Conf., IECON'02*, Vol. 4, 2002, pp. 932–7.

[42] P. Enjeti, and W. Shireen, "An advanced programmed PWM modulator for inverters which simultaneously eliminates harmonics and rejects dc link voltage ripple," *Proc. Applied Power Electronics Conf. and Expo., APEC'90*, 1990, pp. 681–5.

[43] E. Najafi, and A.H.M. Yatim, "Design and implementation of a new multilevel inverter topology," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–54, 2011.

[44] S. Caroline, and M. M. Beno, "Comparison on design and simulation of multilevel inverters," *Solid State Technol.*, vol. 64, no. 2, pp. 905–14, 2021.

[45] G. J. Su, "Multilevel DC-link inverter," *IEEE Trans. Industry Appl.*, vol. 41, no. 3, pp. 848–54, 2005.

[46] S. N. Rao, D. A. Kumar, and C. S. Babu, "New multilevel inverter topology with reduced number of switches using advanced modulation strategies," *2013 International Conference on Power, Energy and Control (ICPEC)*, 2013, pp. 693–9.

[47] M. Easley, M. Shadmand, and H. A. Abu-Rub, "Computationally-efficient optimal control of cascaded multilevel inverters with power balance for energy storage systems," *IEEE Trans. Ind. Electron.*, 2021.

[48] S. N. Rao, P. K. Varanasi, S. K. Anisetty, and B. M. Manjunatha, "Implementation of cascaded H-bridge DC-link inverter for marine electric propulsion drives," *Energy Harvesting and Systems*, 2022. https://doi.org/10.1515/ehs-2022-0049.

[49] S. N. Rao, D. A. Kumar, and C. S. Babu, "Implementation of cascaded based reversing voltage multilevel inverter using multi carrier modulation strategies," *Int. J. Power Electron. Drive Syst.*, vol. 9, no. 1, p. 220, 2018.

[50] S. N. Rao, D. A. Kumar, and C. S. Babu, "Integration of reversing voltage multilevel inverter topology with high voltage gain boost converter for distributed generation," *Int. J. Power Electronics Drive Syst.*, vol. 9, no. 1, p. 210, 2018.