

**Short thesis for the degree of doctor of philosophy
(PhD)**

**Advancements in EEG Signal
Classification: Deep Learning Approaches
and Hardware Implementation on FPGA**

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Contents

1.	Background and aims of the dissertation	1
2.	New results	7
2.1.	Thesis group 1: Review of EEG-based software and hardware solution	7
2.1.1	A Comparative Study of Traditional and New Methods for EEG	7
2.1.2	Integrated Hardware-Accelerated Techniques for Enhanced EEG Signal Processing	11
2.2.	Thesis group 2: Development and optimization of the EEG signal recognition model	17
2.2.1	Determination of optimal frequency feature indicator	17
2.2.2	Exploration of combining traditional EEG processing solutions with CNN	19
2.2.3	Data enhancement algorithm based on EEG signal	20
2.2.4	Exploration of two branch CNN	23
2.3.	Thesis group 3: Hardware Acceleration and Optimization	25
2.3.1.	Optimization plan based on convolutional hardware implementation	25
2.3.2.	Software-configurable lightweight CNN inference accelerator	28
	Publication list	30
	Bibliography	31

1. Background and aims of the dissertation

The human brain is a highly complex system, and understanding its functions is crucial for addressing neurological disorders and enhancing human-machine interaction. As research into the brain progresses, we continually uncover new theoretical insights. This theoretical research not only aids in understanding how the brain works but also provides a new perspective on human cognition. Firstly, it can help diagnose brain diseases earlier and more accurately, generating detailed diagnostic reports to support the development of targeted treatment plans. Secondly, it fosters the integration of neuroscience with related fields such as computer science, information and communication engineering, neuro engineering, psychology, and clinical medicine. This interdisciplinary approach promotes mutual advancement and paves the way for rapid development and theoretical breakthroughs across these disciplines.

In 2013, the United States launched the BRAIN Initiative, aiming to advance research in neuroscience and related brain diseases through innovative neurotechnology. By 2020, the initiative's annual research funding reached \$500 million. Similarly, in 2013, the European Union initiated the Human Brain Project, investing €1 billion to integrate computer technology and neuroscience for in-depth brain research. In 2014, Japan announced the Brain/MINDS project,

dedicating ¥3 billion to studying brain functions and related diseases. Major breakthroughs in brain science and brain-like artificial intelligence could revolutionize human-machine interaction and significantly aid individuals with movement disorders.

A Brain-Computer Interface (BCI) is a computer-based system designed to capture brain activity signals [1]. By processing these signals through operations such as signal processing, feature extraction, and classification, BCIs convert the decoded information into commands for external devices, enabling human-computer interaction. BCI systems typically utilize methods like electroencephalography (EEG), electrocorticography (ECoG), and near-infrared spectroscopy (NIRS) to record brain signals. Among these methods, EEG stands out for its non-invasiveness, affordability, and high temporal resolution, making it widely used in BCI research.

Currently, research on BCI systems is primarily focused on theoretical and experimental aspects, though some advanced technologies are ready for clinical trials. As an emerging field, BCI systems have vast application prospects in several areas:

- **Neuroscience Research [1]:** BCI systems can capture electrical signals generated by brain activity and decode them using machine learning algorithms to analyze brain signals. As an important interdisciplinary research direction, BCI technology can integrate and improve existing methods, further promoting the development of neuroscience and related disciplines.

- **Clinical Medical Rehabilitation [2]:** BCI technology can assist individuals with motor disabilities in rehabilitation training, helping them regain control over their limbs. By processing and converting brain signals, users' movements or intentions can be translated into commands to control assistive devices like wheelchairs and robotic arms, facilitating interaction between users and the external world and addressing some of their challenges.
- **Entertainment [3]:** BCI technology can be combined with virtual reality to create unprecedented entertainment experiences. It provides an immersive virtual reality environment, offering users a more engaging human-computer interaction.
- **Smart Home [4]:** With the rapid development of communication and IoT technologies, BCI can be widely applied in daily life. BCI-based smart homes can synchronize with human emotions, enhancing quality of life.
- **Transportation and Military [5]:** BCI technology, when integrated with smart driving technologies, enables remote control of vehicles and aircraft. Combined with intelligent robotics, BCI can allow machines to perform hazardous tasks. In the military, BCI can use brainwave information for encryption and more efficient coordinated operations.

In summary, BCI technology is at the forefront of brain science and brain information processing research, offering high scientific

value and extensive application prospects. As a multidisciplinary frontier technology, BCI integrates advanced engineering techniques and methods, significantly promoting the development of neuroscience and related fields, and plays a crucial role in understanding brain cognitive mechanisms, diagnosing, and treating brain diseases.

Despite significant performance improvements in brain-computer interface (BCI) systems in recent years, researchers still face numerous challenges in promoting BCI technology. One major issue is that the current performance of BCI systems remains relatively low compared to traditional input methods, making them insufficient for supporting fast and complex communication and control. This performance bottleneck is mainly due to an incomplete understanding of the neural mechanisms underlying information encoding in brain signals. Furthermore, decoding EEG signals requires more efficient computational modeling methods, including advanced signal processing and machine learning techniques. Given these various open challenges, real-world BCI systems are still in their infancy. Designing a practical and effective BCI system primarily involves addressing the following challenges:

1. EEG signals offer a direct window into brain activity, but decoding motor intentions from these signals is complex due to their inherent high dimensionality, variability, and noise.

2. The large amount of EEG data generated during experiments requires efficient processing and classification techniques. This process often relies on manual operations, and data preprocessing (such as filtering and denoising), parameter selection (such as frequency bands and time windows), and feature engineering (including feature extraction and selection) are complex and time-consuming, heavily dependent on expertise in the field.
3. The advent of deep learning techniques, especially convolutional neural networks (CNNs), has led to significant advancements in fields like computer vision and natural language processing. However, CNNs require large sample datasets to support their learning efficacy, and EEG signals are typically considered a small dataset. This often leads to overfitting when deep learning is applied to EEG signal processing.
4. While CNNs have achieved promising results in motor imagery recognition, deploying these models in real-time applications presents computational challenges. Real-time processing is crucial for BCI systems to provide timely feedback and enable seamless interaction. However, deep learning models, particularly CNNs, are computationally intensive and require powerful processing capabilities, which can be a bottleneck in real-time applications.

We aim to address these challenges by exploring new methods for EEG signal processing, feature extraction, classification, and hardware acceleration.

This dissertation presents a total of eight theses, categorized into three groups:

Thesis Group 1: Review of EEG-based Software and Hardware Solutions.

Thesis Group 2: Development and Optimization of the EEG Signal Recognition Model.

Thesis Group 3: Hardware Acceleration and Optimization.

2. New results

2.1. Thesis group 1: Review of EEG-based software and hardware solution

2.1.1 A Comparative Study of Traditional and New Methods for EEG

In [J2], we explore various pre-processing techniques such as Independent Component Analysis (ICA) and Principal Component Analysis (PCA), followed by feature extraction methods like Power Spectrum Density and Wavelet Transform. Finally, we will review classification algorithms including Artificial Neural Networks (ANN) and Support Vector Machines (SVM). We also made a comparison table based on the advantages and disadvantages of each technology so that researchers can choose the appropriate technology according to their task requirements.

Since EEG signals are very weak physiological signals, typically in the microvolt range, they are highly hurt by artifacts such as eye blinks, muscular activity, and electrical grounding disturbances. These interference signals significantly complicate EEG signal processing and elevate the computational demands for further analysis. Table 2.1 offers a comparison of these methodologies.

Table 2.1 Comparison of the pre-processing methods

Approach	Advantages	Disadvantage
ICA	● High calculation efficiency ● Works well for large data sized	● Require more computational for decomposition
PCA	● Reduction of feature dimension	● May lost critical information on non-principal components
CAR	● The best among all the reference methods	● Needs sufficient head coverage
CSP	● Good effect on EEG data processing based on motor imagination ● does not need to select a specific frequency band in advance.	● sensitive to noise ● needs to be used with multiple electrodes
Adaptive Filtering	● Good for the signals with overlapping spectra	● Needs two signals (including reference signal)
Digital Filter	● Easily remove electrical grounding noise	● Requires EEG signal and artifact occupy distinct frequency bands

Feature extraction plays a pivotal role in the EEG signal processing process by transforming EEG data into a set of relevant features that can be more easily and effectively analyzed[6]. Its purpose is usually noise reduction, dimensionality reduction, highlighting relevant patterns, etc. The extracted features serve as the input for machine learning algorithms and classifiers. Carefully selected and validated features ensure that the model performs well

across different tasks and conditions. Table 2.2 provides a comparison of various extraction methods.

Table 2.2 Comparison of extraction approaches

Approach	Advantages	Disadvantages
PSD	● Feature stability ● Applicable for stationary signals	● Not suitable for unstable signals ● Unable to analyze time-domain signals
PCA	● Lossless dimension reduction	● Unable to process complicated set of data
ICA	● fast calculation speed ● high efficiency	● Require more computational for decomposition
AR	● Require short duration of data ● Reduce spectra loss problems and give better frequency resolution	● Not available for stationary signals
WT	● Works well for nonstationary signals ● Can analyze signal in time and frequency domain	● Lacking of specific methodology to apply to pervasive noise
WPT	● Works well to analyze the nonstationary signals ● provide precise frequency resolution	● Increase computational time

Classification is a fundamental task in data processing and machine learning. It trains network to assign data points to predefined categories or classes. Another purpose is prediction. It applies the

training model to new data and classifies it as one of the predefined categories. A comparative analysis of these classification methods is presented in Table 2.3.

Table 2.3 Comparison of the classification methods

Approach	Advantages	Disadvantages
ANN and DL	● High accuracy ● flexible structure	● Performance depends on the number of neurons in the hidden layer
K-NN	● Easy to understand, ● simple to implement	● Sensitive to irrelevant and redundant features ● requires large storage space
LDA	● Easy to use ● Low computational complexity	● Requires a linear model
SVM	● Performance is better compare to other linear classifiers	● Low computational complexity
NB	● Easy to understand	● Independent variables
DT	● High interpretability ● Ease of use	● Limited expressiveness ● Easy overfitting

***Thesis 1:** I bring together the latest advancements in EEG signal processing and classification, offering a comprehensive and insightful review of both traditional and state-of-the-art techniques. Additionally, my work highlights the growing significance of deep*

learning in the field of EEG analysis and emphasizes the need for further exploration and development of deep learning algorithms.

The result has been published to Carpathian Journal of Electronic & Computer Engineering with title “A Review of Processing Methods and Classification Algorithm for EEG Signal[J2].”

2.1.2 Integrated Hardware-Accelerated Techniques for Enhanced EEG Signal Processing

As the importance of EEG spreads over many fields, the demand for fast data processing solutions is growing. Researchers aim to revolutionize this field by substantially enhancing computational efficiency and classification precision. While [J2] covered numerous EEG-based data processing technologies, [J5] focuses on the hardware solutions for implementing these technologies. We explore hardware solutions designed for pre-processing, feature extraction, and the different types of features. Based on the existing processing methods of EEG signals, we divide them into five categories of features: frequency-based, time-based, time-frequency, spatial, and raw signal. A summary of the reviewed articles is presented in Table 2.4.

Table 2.4 Feature Extraction Methods

Feature domain	Authors	Algorithm	Work Description
Frequency-based	[7] [8]	PSD	A power spectrum approximation per channel

		Hardware friendly, no FFT accelerator required Easily lose band information
	[9]	PSD Dataset: Own FEXD Hardware: Digilent Atlys with Spartan-6 A FFT Accelerator with 128 frequency bins Suitable for capturing fluctuations within and between brainwave frequency bands
	[10]	CFC Use connection diagrams to represent EEG Reduces the need to store and compute EEG CORDIC is required to calculate the Hilbert transform of each frequency band
Time-based	[11]	HOC, SK Hardware: TSMC 0.18um 1P6M CMOS chip Databases: DEAP and SEED Use ASKI to reduce gate counts, 3-bit SR triggers
	[12]	Hjorth parameters Hardware: Zynq-7000 FPGA Dataset: Bonn University EEG database Classifier: KNN

	[13] [14]	SE	For statistics, complexity and irregularity system More suitable for short and noisy datasets Relatively hardware- friendly
Time- Frequency	[15]	STFT	Hardware: Xilinx Zedboard Extracted 20 features from 128 channels
	[16]	STFT	Used for epilepsy detection Only simulation, not applied to real FPGA chips
	[17]	STFT	Hardware: ADVANTEST V93000 PS1600 chip Dataset: DEAP STFT features mixed with asymmetric indices
	[18]	DWT	Hardware: Basys 3 Artix-7 FPGA Board Classifier: LDA Suitable for developing low-cost, marketable products
	[19]	CWT	Hardware: Spartan 3AN FPGA Efficient Morlet wavelet function architecture trade-off between speed and silicon area
Spatial	[20]	CSP	Hardware: Altera FPGA platform (Stratix-IV) Dataset: motor imagery in BCI competition

		Classifier: MD Time delay of 0.5 seconds
	[21] CSP	Improve of [20], reducing the delay to 0.399s
	[22] SCSSP	Hardware: Virtex-6 FPGA Dataset: BCI Competition IV-dataset 2a Classifier: SVM
	[8] Asymmetric indices + PSD	Based on a scaled version of IHPR with a customized LUT
	[7] Asymmetric indices + PSD	Improve of [8], LIHPR reduces the gate counts and power consumption then IHPR
	[23] DTF	Used to describe the incidental effect of one EEG channel on another channel at a specific frequency Difficult to implement in hardware as it requires calculation of the transfer matrix, square roots and division of the multivariate autoregressive model
Raw	[24] PSD CNN	Dataset: Own For emotion recognition and fatigue-driving

CNNs have demonstrated remarkable capabilities in EEG classification. It established them as a dominant force in the software-driven deep learning field. Despite their excellence in feature learning and classification, CNNs often require substantial computational resources, especially for real-time applications like BCI. To address these demands, we reviewed five highly efficient CNN hardware techniques specifically applied to EEG signal processing: pruning, quantization, tensor decomposition, knowledge distillation, and neural architecture search. The applications of these techniques in EEG signal processing are summarized in Table5.

Table 2.5 List of Collected CNN Hardware Techniques

Method	Authors	Work Description
Weight Pruning	[25], [26]	Hessian matrix of the loss function
	[27], [28]	Three-step method
	[29]	Frequency-domain approach
	[30]	Variable compression rates
	[31]	GMM
	[32]	Energy reduction with compression ratios and accuracy loss
Structural Pruning	[33], [34], [35]	Criterion-Based Pruning
	[36]	Ranking-Based Pruning
	[37], [38]	Optimization-Based Pruning
	[39], [40], [41]	Whole-layer pruning methods
	[42], [43], [44]	Automatically identify and prune

Quantization	[45]	Characterized by even step sizes
	[46]	Represented by logarithmic distributions
	[47], [48]	Post-training quantization
	[49], [50], [51]	Quantization-aware training
Low-Rank Matrix Decomposition	[52]	Decompose the product of weight matrices and input data
	[53]	Sparsity: Maintaining a lower rank for less critical neurons
	[54]	Channel-wise SVD decomposition by dividing kernels into two layers
	[55]	Low-rank approximation without invoking SVD at every training step
	[56]	Joint matrix factorization scheme
Tensorized Decomposition	[57]	Tucker decomposition
	[58], [59]	CANDECOMP/PARAFAC (CP)
	[60], [61], [62]	Tensor Train decomposition
	[63]	Tensor Ring decomposition
Knowledge Distillation	[64], [65], [66], [67]	Offline distillation
	[68], [69], [70]	Online distillation
	[71], [72], [73]	Self-knowledge distillation
Neural Architecture Search Space	[74]	NASNet
	[75]	ENAS
	[76]	AutoDispNet
	[77]	MnasNet

Neural	[78]	NAS-RL
Architecture	[79]	MetaQnn-RL
Search Algorithm	[80]	Optimizing neural structures
Neural	[81]	Progressive NAS
Architecture	[82]	ReNAS
Search	[83]	One-Shot NAS
Performance	[84],	Hardware-aware NAS
Evaluation	[85],	
Strategy	[86], [87]	

***Thesis 2:** I provided a comprehensive review of various state-of-the-art EEG-based hardware solutions, emphasizing pre-processing and feature extraction stages, and hardware convolutional neural network acceleration techniques for EEG signal processing, focusing on efficiency and performance improvements.*

The result has been published to Sensors Journal with title “A Comprehensive Review of Hardware Acceleration Techniques and Convolutional Neural Networks for EEG Signals[J5].”

2.2. Thesis group 2: Development and optimization of the EEG signal recognition model

2.2.1 Determination of optimal frequency feature indicator

We first use the EEGLAB toolbox to analyze the spectrum of eye open and eye close states. We found the “alpha blocking[88]“ phenomenon. Alpha (8-13Hz) waves emerge when

individuals are awake, serene, and with their eyes closed. However, upon opening their eyes, engaging in cognitive tasks, or receiving stimuli, alpha waves fall and transition into faster waves. It reappears when the individual regains calmness and closes their eyes again. This obvious feature makes the alpha band the research object of most researchers.

We used the power spectral density method to extract the EEG data of 50 participants from PhysioNet EEG Database in [C2]. The feature data of beta band (13-32Hz) and alpha band were inputted into a double hidden layer MLP network respectively. The results show that the average accuracy of using the beta band as input is 4.2% higher than that of using the alpha band.

***Thesis 3:** I found that it would be reasonable to use the beta wave as an EEG analytical indicator. There was no significant difference in the training results when using alpha or beta features individually. And combining both features simultaneously improved accuracy.*

The result has been published to 1st Conference on Information Technology and Data Science with title “Comparison of EEG Data Processing Using Feedforward and Convolutional Neural Network[C2].”

2.2.2 Exploration of combining traditional EEG processing solutions with CNN

We know from [C2] that CNN achieves good accuracy when using raw data as input. We wonder if we can get better results if we use other manually extracted features as input. Short-Time Fourier Transform (STFT) and Continuous Wavelet Transform (CWT), as a time-frequency analysis technique, have been widely used in EEG signal processing. We developed a custom interface using MATLAB to ensure that we could collect high-quality EEG data with minimal noise from a consumer-grade OpenBCI device. CWT and STFT techniques are used to preprocess the collected data respectively. The preprocessed data and the raw data are respectively input into three CNNs with similar network structures. After turning the hyperparameters of the CNNs to best process this data, the network achieved an accuracy of 91.23%, in contrast to 89.17% and 90.21% for recognition accuracy using the raw data directly and STFT processing, respectively.

***Thesis 4:** I have shown that using manually extracted features as input to convolutional neural networks can steadily improve the accuracy of the algorithms in all time windows. Among them, continuous wavelet transform has the best effect, with an accuracy of 91.23%.*

The result has been published to Electronics Journal with title “FPGA-Based Hardware Accelerator on Portable Equipment for EEG Signal Patterns Recognition[J1].”

Preprocessing Type	Segment Size (Seconds)	Mean Accuracy	Best Accuracy
Raw	0.25	74.87%	78.30%
	0.5	78.26%	84.00%
	1	83.23%	89.92%
	1.5	83.46%	88.36%
	2	84.33%	89.21%
	2.5	83.25%	89.76%
	3	84.72%	89.17%
STFT	0.25	74.91%	78.12%
	0.5	79.33%	84.92%
	1	85.12%	87.33%
	1.5	84.20%	88.16%
	2	85.72%	88.99%
	2.5	85.39%	89.23%
	3	85.52%	90.21%
CWT	0.25	75.22%	80.54%
	0.5	80.21%	86.06%
	1	85.55%	89.92%
	1.5	85.76%	89.28%
	2	86.33%	91.31%
	2.5	86.25%	91.65%
	3	86.72%	91.23%

Figure 2.1 The comparison performance of different preprocessing functions

2.2.3 Data enhancement algorithm based on EEG signal

In [J1], we found that the generalization problem of SoftMax was caused by the small dataset. We try to address this problem by increasing the number of samples. In the field of computer vision, there are already some common Data Augmentation (DA) methods, such as rotation, cropping, deformation, and scaling. Based on our previous analysis of the basic properties of EEG signals, we can find that EEG signals exhibit different characteristics in both the time domain and the frequency domain. Therefore, simple data enhancement methods may not be applicable to EEG signals. Current

EEG signal data augmentation techniques can be broadly classified into two main categories: data transformation [89-91] and noise addition [92, 93]. Data transformation involves modifying the existing signals to create new samples. This can include techniques such as time-warping, window slicing, or signal filtering. These methods aim to simulate variations in the signal that might naturally occur, enhancing the model’s ability to generalize from the training data. Noise addition, on the other hand, involves incorporating various types of noise into the EEG signals to make the model more robust to real-world conditions. This can include adding Gaussian noise, salt-and-pepper noise, or other perturbations that mimic potential interferences during signal acquisition.

We propose an EEG DA method based on the time-frequency domain. Our method adds a large number of artificial samples by randomly exchanging sample data in the time and frequency domains to remain the characteristics of the original EEG signal to the greatest extent possible. We iterated 1000 times to generate 1000 fresh samples. The testing dataset is BCI Competition IV Data Set 2a. Consequently, the total number of samples for each subject increased from the initial 576 to 1576. We tested VGGNet, EEGNet, and our proposed CNN structure in [J1]. As shown in Table 2.6, our DA technology has different degrees of improvement in different models.

Table 2.4 Compared results with EEGNet and VGGNet, marked with the suffix (_A) indicates the application of DA techniques

Subject No.	Acc(%)					
	VGGNet	VGGNet_A	EEGNet	EEGNet_A	Our	Our_A
1	79.32	85.36	88.21	91.33	97.23	98.61
2	69.01	77.22	70.35	72.58	94.77	98.29
3	91.11	92.67	92.40	93.14	94.12	97.99
4	68.32	66.12	81.26	85.65	95.22	97.1
5	59.00	70.15	85.77	83.85	93.25	96.72
6	70.32	71.39	73.12	76.98	92.36	96.37
7	82.55	85.73	93.10	98.54	94.8	97.69
8	79.33	88.52	90.73	89.32	95.75	97.22
9	70.74	72.29	91.05	89.99	96.38	98.51
Mean	74.41	78.82	85.11	86.82	94.88	97.61

Thesis 5: I demonstrated that our data augmentation method shows significant accuracy improvements for multiple models, including VGGNet, EEGNet, and two branch CNN architectures, with average enhancements of up to 4.41% and 11.15% for individual subjects.

The result has been published to Sensors Journal with title “Classification of Motor Imagery EEG Signals Based on Data Augmentation and Convolutional Neural Networks[J3].”

2.2.4 Exploration of two branch CNN

In [J1], we found that CNN with CWT feature maps as input has good accuracy. At the same time, we note that there are performance differences between different preprocessing techniques and segment sizes. We speculate that the classification accuracy can be further improved by using branch learning methods. That is, each branch learns different features separately. The two branch structure we used can be found in [J4]. We designed two branch CNN of different scales for time domain and CWT mapping to achieve more comprehensive feature extraction. The average accuracy of this method reached 97.61%, the highest among all models, as shown in Table 2.6 and Table 2.7. Figure 2.3 briefly explains the implementation of other models. We believe this technology has the potential to be applied to other machine learning and MI-EEG analysis tasks, and we look forward to further exploring its capabilities.

Literature	Classifier	Contribution
HS-CNN [37]	CNN	- Different convolution kernel scales are designed for EEG signals in different frequency bands, and convolution operations are performed in the temporal and spatial dimensions using one-dimensional convolution kernels. - Identically labeled samples are segmented and then swapped and recombined, then divided by frequency bands, and different segments of the same frequency band are swapped and recombined.
PSO-CNN [46]	CNN	- The signal is input to the CSP filter, while the PSD of different frequency bands is calculated, and the particle swarm optimization algorithm is introduced for feature optimization. - CNN has only one convolutional layer.
CNN-LSTM [47]	CNN+LSTM	- Using the Filter Bank Common Spatial Pattern technique - Hybrid network to extract multimodal features.
DWT-CNN [48]	CNN	- Sliding window for data enhancement, calculating PSD for optimal frequency bands. - Decompose 3×3 convolution kernels into 4×1 or 2×1.

Figure 2.3. Contribution to comparative literature.

Table 2.5 Compare the table of the proposed method with state-of-the-art methods

Subject No.	Acc(%)					
	HS-CNN	PSO-CNN	CNN-LSTM	DWT-CNN	Our	Our_A
1	90.07	93.30	98.82	98	97.23	98.61
2	80.28	84.59	98.64	98	94.77	98.29
3	97.08	91.68	96.92	95	94.12	97.99
4	89.66	84.55	96.50	96	95.22	97.1
5	97.04	86.54	92.75	86	93.25	96.72
6	87.04	76.92	91.84	92	92.36	96.37
7	92.14	94.03	95.07	94	94.8	97.69
8	98.51	93.20	95.25	93	95.75	97.22
9	92.31	92.24	99.23	98	96.38	98.51
Mean	91.57	85.56	96.13	94	94.88	97.61

***Thesis 6:** I demonstrated that the proposed two-branch CNN structure achieves 97.61% accuracy, which is the best classification accuracy in comparison with popular EEG models (VGGNet and EEGNet) and other state of art models. Meanwhile, support vector machine with convolutional neural networks is the best classification method with a small amount of training sample data, outperforming decision trees and Softmax.*

The result has been published to Sensors Journal with title “Classification of Motor Imagery EEG Signals Based on Data Augmentation and Convolutional Neural Networks[J3],” and “Enhancing Motor Imagery Classification in Brain–Computer Interfaces Using Deep Learning and Continuous Wavelet Transform[J4].”

2.3. Thesis group 3: Hardware Acceleration and Optimization

2.3.1. Optimization plan based on convolutional hardware implementation

The Xilinx High-Level Synthesis (HLS) Suite allows conversion of C, C++ or SystemC to RTL implementation. Compared to traditional hardware description languages (VHDL or Verilog), HLS significantly reduces the required code and enhances efficiency of Vivado intellectual property (IP) design. Therefore, we used HLS

instead of Verilog to program the CNN circuit. It is important to note that not all C and C++ syntax is supported by HLS [94].

Since the convolution layer is the most computationally intensive block in a CNN, our main work is to optimize the calculation of the convolution layer. In order to improve the computational efficiency of the convolutional layer, it is very important to utilize the parallel computing capabilities of FPGA. Unrolled loops facilitate multiple independent operations simultaneously rather than sequentially processing a single set of operations[95]. In general, loops in C/C++ functions remain rolled. So the synthesis creates the logic for one iteration of the loop, and the RTL design executes this logic for each iteration in sequence by default. UNROLL pragma transforms loops by generating multiple copies of the loop body in the RTL design, allowing several or all loop iterations to occur in parallel. We found that the loop dimensions of “Number of output feature map” and “Input image depth” are suitable for unrolling. Because they are data-independent variables in the convolution loop operation.

The result of the expansion increases the consumption of FPGA on-chip resources, but the latency and interval are reduced by 7.7 times, as shown in Table 2.9.

In addition, we selected the LetNet-5 network for horizontal comparison with other FPGA designs to demonstrate the superiority of the proposed system, as shown in Table 2.10.

Table 2.9 The utilization of convolution computing function before and after optimizing.

Name	After	Before
BRAM	8	5
DSP48E	20	5
Flip-flops	3209	623
Look-up tables	3573	1364
Latency	48,237	374,368
Interval	48,237	374,368

Table 2.10 The comparison with some predecessors.

Metric	Our Design	[96]	[97]
Model	LeNet-5	LeNet-5	LeNet-5
Programming language	HLS	Verilog	Verilog
Data type	32 bits float	32 bits float	12 bits fixed
Operation frequency	100 MHz	100 MHz	100 MHz
BRAM	264	2	45
DSP48E	62	23	158
Flip-flops	8947	11962	2772
Look-up tables	9334	9893	4254
Accuracy	98.34%	98.2%	97.59%
Inference time	0.17 s	0.653 s	0.143 s

Thesis 7: *I have shown that the latency after the Optimization was reduced by 7.7 times. By comparing with other FPGA -based CNN design, the inference speed of our design is faster and has less resources consumed.*

The result has been published to Electronics Journal with title “FPGA-Based Hardware Accelerator on Portable Equipment for EEG Signal Patterns Recognition[J1].”

2.3.2. Software-configurable lightweight CNN inference accelerator

Hardware implementation of CNNs presents numerous challenges due to their computational intensity and complexity. In [J6], we have learned about many hardware implementation methods of CNN inference accelerators and studied its development trend. GPU platforms are often the preferred choice for this purpose because of their excellent computing performance and user-friendly development environment. However, GPUs have universal applicability limit due to its high cost, high power consumption, and large physical size. Instead, FPGA-based inference accelerators have the potential to surpass GPUs in terms of both CNN computing performance and power efficiency. This aligns with our goals for improving the practical implementation of CNNs.

Traditional FPGA development involves several meticulous and time-consuming steps, including HDL coding, simulation, synthesis, implementation, and bitstream generation. These stages require significant effort and can be particularly cumbersome due to their iterative nature. Furthermore, with the rapid advancements and frequent updates in Convolutional Neural Network (CNN) models, researchers often need to test new models repeatedly, necessitating a re-execution of these development steps each time. This repetitive process leads to substantial time wastage for researchers.

To address these challenges, we aim to develop a design framework that allows for the modification of the CNN network

structure at the software level. By enabling network reconfiguration through software, we can streamline the development process, significantly reducing the time and effort required to test new CNN models on FPGA platforms. We developed an inference accelerator for lightweight CNNs and conducted experiments on the PYNQ-Z2 development board. We first selected the CNN introduced in [J1] for verification. The result is shown in Table 2.8

Table 2.8 The comparative performance of different platforms

Hardware Platform	CPU	Accelerator	Memory	Inference Time	Accuracy	Power	Power Efficiency	Price	Weight
Laptop	Intel Core i5-7300HQ @ 2.50 GHz	GTX 1050Ti @ 1620 Mhz	8 GB DDR4 @2666 MHz	0.003 s	89.92%	131.1 W	2.5	~\$750	3.61 kg
PYNQ-Z2	ARM Dual-core Cortex A9 @ 650 MHz	-	512 MB DDR3 @525 MHz	5.1 s	89.85%	1.9 W	0.1	~\$177	0.22 kg
PYNQ-Z2	ARM Dual-core Cortex A9 @ 650 MHz	FPGA @ 100 Mhz	512 MB DDR3 @525 MHz	0.22 s	89.69%	3.1 W	1.46	~\$177	0.22 kg

Thesis 8: *I demonstrated that Our accelerator is not only 16 times faster than traditional CPU-based inference in edge computing scenarios but also achieves a remarkable energy efficiency ratio, being 14.6 times more efficient than CPUs in such applications. Moreover, our accelerator is highly flexible, allowing researchers to modify the CNN structure at the software level without requiring any hardware changes.*

The result has been published to International Conference on e-Health and Bioengineering (EHB) with title “Hardware Implementation of CNN Based on FPGA for EEG Signal Patterns Recognition[C1].”

Publication list

- [J1] Xie, Yu, Tamás Majoros, and Stefan Oniga. “FPGA-Based Hardware Accelerator on Portable Equipment for EEG Signal Patterns Recognition.” *Electronics* 11.15 (2022): 2410.
- [J2] Xie, Yu, and Stefan Oniga. “A Review of Processing Methods and Classification Algorithm for EEG Signal.” *Carpathian Journal of Electronic & Computer Engineering* 12.3 (2020).
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Registry number:
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PhD Publication List

Candidate: Yu Xie

Doctoral School: Doctoral School of Informatics

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List of publications related to the dissertation

Foreign language scientific articles in international journals (5)

1. **Xie, Y.**, Oniga, I. L.: A Comprehensive Review of Hardware Acceleration Techniques and Convolutional Neural Networks for EEG Signals.
Sensors. 24 (17), 1-28, 2024. ISSN: 1424-8220.
DOI: <http://dx.doi.org/10.3390/s24175813>
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2. **Xie, Y.**, Oniga, I. L.: Enhancing Motor Imagery Classification in Brain-Computer Interfaces Using Deep Learning and Continuous Wavelet Transform.
Appl. Sci.-Basel. 14 (19), 1-16, 2024. ISSN: 2076-3417.
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3. **Xie, Y.**, Oniga, I. L.: Classification of Motor Imagery EEG Signals Based on Data Augmentation and Convolutional Neural Networks.
Sensors. 23 (4), 1-16, 2023. EISSN: 1424-8220.
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4. **Xie, Y.**, Majoros, T., Oniga, I. L.: FPGA-Based Hardware Accelerator on Portable Equipment for EEG Signal Patterns Recognition.
Electronics (Switzerland). 11 (15), 1-15, 2022. EISSN: 2079-9292.
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Foreign language conference proceedings (3)

6. **Xie, Y.**, Oniga, I. L.: Cross-task EEG signal classification method based on transfer learning.
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8. **Xie, Y.**, Majoros, T., Oniga, I. L.: Hardware Implementation of CNN Based on FPGA for EEG Signal Patterns Recognition.
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List of other publications

Foreign language scientific articles in Hungarian journals (1)

9. Majoros, T., Oniga, I. L., **Xie, Y.**: Motor imagery EEG classification using feedforward neural network.
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Foreign language scientific articles in international journals (1)

10. **Xie, Y.**, Buchman, A.: A survey for Communication security of the embedded system.
CARPAT H J ELECTRONIC COMPUTER ENGINEERING. 14 (2), 15-19, 2021. EISSN: 2343-8908.
DOI: <http://dx.doi.org/10.2478/cjece-2021-0009>

Total IF of journals (all publications): 12,3

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