

# ON THE DESIGN OF CLASS-J MICROWAVE POWER AMPLIFIER

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Due to the ISM band being unlicensed for communication applications, a lot of applications have been developed in this band and a good example is WiFi IEEE 802.11a,b,g,n of Bluetooth. This numeracy of applications motivated this paper. The paper is concerned with the design of a low distortion 20 dBm 2.4 GHz class-J power amplifier (PA) since PAs are indispensable in radio communications. The design is based on the AVAGO ATF-52189 transistor with a transition frequency of 6 GHz. The design is done as a hybrid circuit network realized using microstrip elements and surface mount device (SMD) capacitors. The schematic design and simulation are carried out using Keysight's Advanced Design System version 2016.01. The simulated PA exhibited a drain efficiency of 69% and a power output of 21 dBm.

**Keywords:** power amplifier, design, ADS

## 1. Introduction

Modern communication systems have evolved over the recent past and are still evolving largely in favor of wireless links especially at the last hop, i.e. the access network. This is majorly because of the demand for mobility.

Wireless communication operates in the radio frequency (RF) range. The notation RF, radio frequencies, actually implies frequencies at which electromagnetic (EM) radiation is practical for communication purposes. These frequencies range from about 3 kHz to about 300 GHz.

A very recent concept is the internet of things that arguably increases the demand for wireless communication by orders of magnitude. It is justifiably estimated that the number of smart devices connected to communication networks will far outnumber the human population in a few years' time.

This demand means that the PA designer at RF frequencies has to keep PAs performing exceptionally well especially in terms of bandwidth and efficiency.

Wide bandwidth is required to support the various applications, services and capabilities from new mobile equipment. Obviously mobile equipment is battery powered and this makes power efficiency a very crucial consideration in RFPA design.

The power amplifier has a power output that necessarily far outweighs the input power driving the amplifier. Strictly speaking however, there is no such thing as power amplification and a more accurate description would be that a 'PA' is really an AC controlled DC to AC power converter.

PAs differ from small signal amplifiers by way of quality and quantity of signal emphasized by the designer. Small signal amplifier designers are concerned with low noise and low distortion amplification, i.e. linear amplification. In short, small signal amplifier designers are obsessed with linearity. PA designers, on the other hand, seek to maximize power output as efficiently as possible even at the expense of linearity. The load line matching concept at the output is therefore preferred to conjugate matching. Aptly then, PA designers are obsessed with power efficiency. Recent works on PA design can be found in [1–5].

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## 2. Design methodology

### 2.1. Active device

The ATF-52189 GaAs transistor was selected as the active device in the amplifier design. From the man-

ufacturer AVAGO Technologies, the datasheet was obtained from which some of the important absolute maximum ratings were extracted and are illustrated in Fig. 1.

Symbol	Parameter	Units	Absolute Maximum
$V_{ds}$	Drain-Source Voltage <sup>[2]</sup>	V	7
$V_{gs}$	Gate-Source Voltage <sup>[2]</sup>	V	-5 to 1.0
$V_{gd}$	Gate Drain Voltage <sup>[2]</sup>	V	-5 to 1.0
$I_{ds}$	Drain Current <sup>[2]</sup>	mA	500
$I_{gs}$	Gate Current	mA	46
$P_{diss}$	Total Power Dissipation <sup>[3]</sup>	W	1.5
$P_{in\ max}$	RF Input Power	dBm	+27
$T_{ch}$	Channel Temperature	°C	150
$T_{stg}$	Storage Temperature	°C	-65 to 150

Thermal Resistance <sup>[2,4]</sup>	
$\theta_{ch-b} = 52^{\circ}\text{C/W}$	

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assuming DC quiescent conditions.
3. Board (package belly) temperature  $T_B$  is 25°C. Derate 19.25 mW/°C for  $T_B > 72^{\circ}\text{C}$ .
4. Channel-to-board thermal resistance measured using 150°C Liquid Crystal Measurement method.

Fig. 1. ATF-52189 absolute maximum ratings

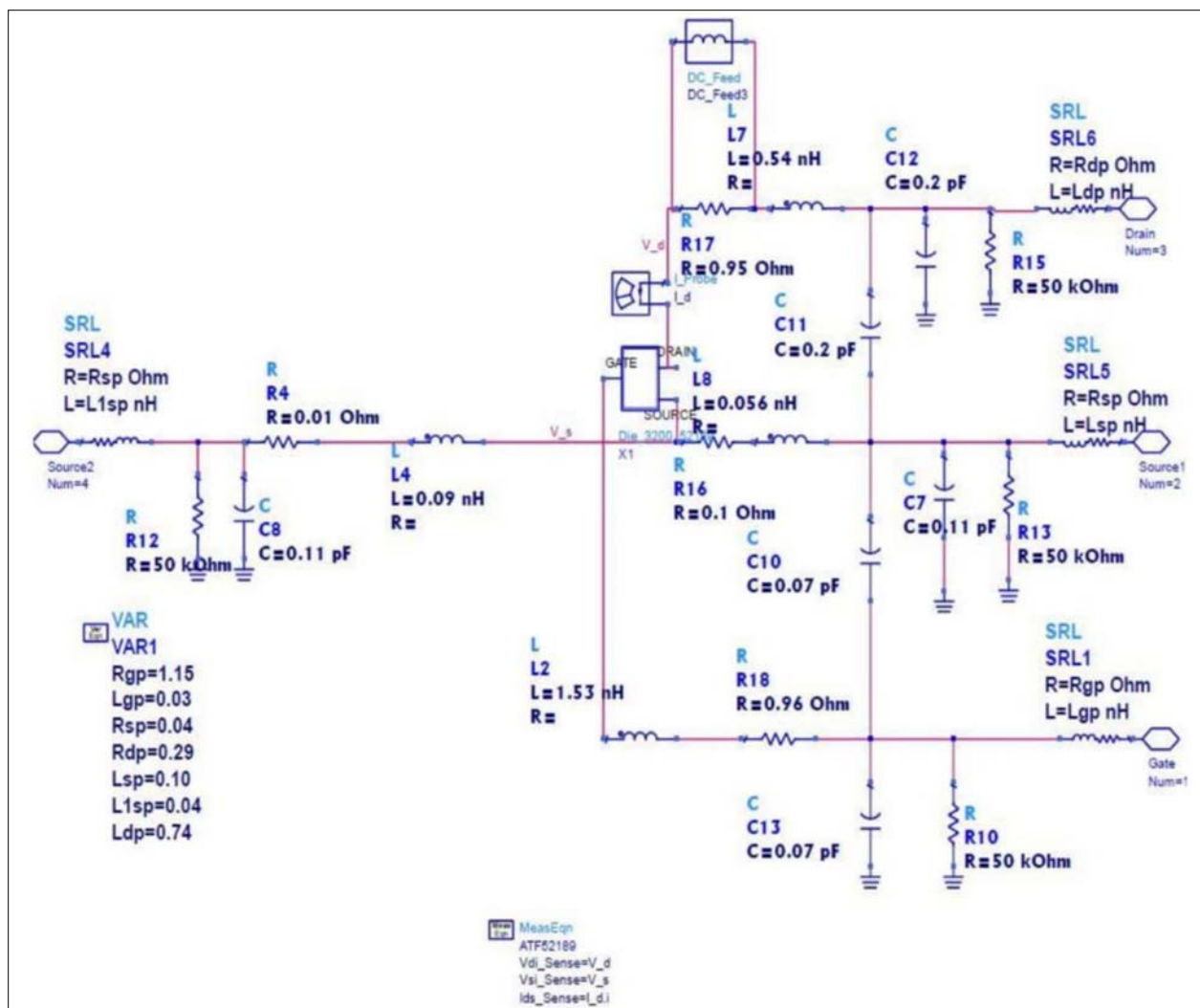


Fig. 2. Extrinsic model of the ATF-52189 obtained from AVAGO Technologies

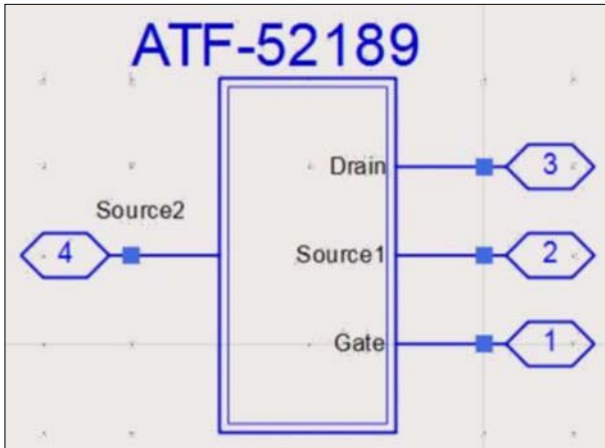


Fig. 3. Schematic symbol of the ATF-52189

## 2.2. Active device nonlinear model

An open parasitic model of the packaged ATF52189 was obtained from the manufacturer as an ADS schematic hierarchy illustrated in Figs 2–4.

## 2.3. DCIV characteristics and waveform prediction from a class-B load-line

The schematic for obtaining the DCIV characteristics is illustrated in Fig. 5. From the DCIV character-

istics, a class-B load-line was constructed from which the voltage swing and current swing were obtained. Based on these swings, class-J waveforms were predicted and plotted. The requisite fundamental and second harmonic impedances were obtained by Fourier techniques. These were the target impedances to be presented to the intrinsic drain of the device. Figs 3–5 illustrate the data display.

## 2.4. Parasitic tune

The impedances obtained from the load line are required at the device intrinsic node, therefore, we expect different load terminations at the extrinsic (package) node. For this reason, a parasitic tune was carried out as shown in Fig. 6. Here, an equation based ideal load was presented at the output and a low power source was connected to the input of the biased device. Using harmonic balance simulation, we swept the ideal load over reasonable impedance values. The resultant intrinsic impedance was calculated from voltage and current measured at the intrinsic node.

By data display methods, the appropriate external loads for the target internal fundamental, second and third harmonic impedances were found.

To improve the tune, the input was conjugate matched to a 50 ohm source and the input power

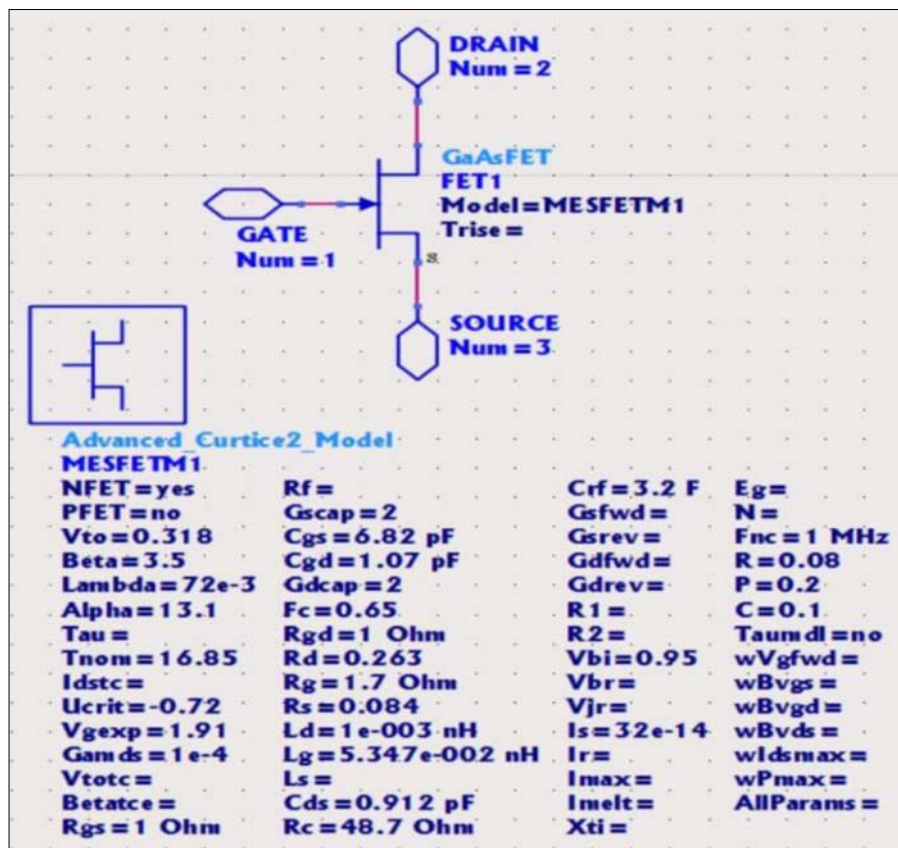


Fig. 4. Intrinsic model of the ATF-52189 obtained from AVAGO Technologies

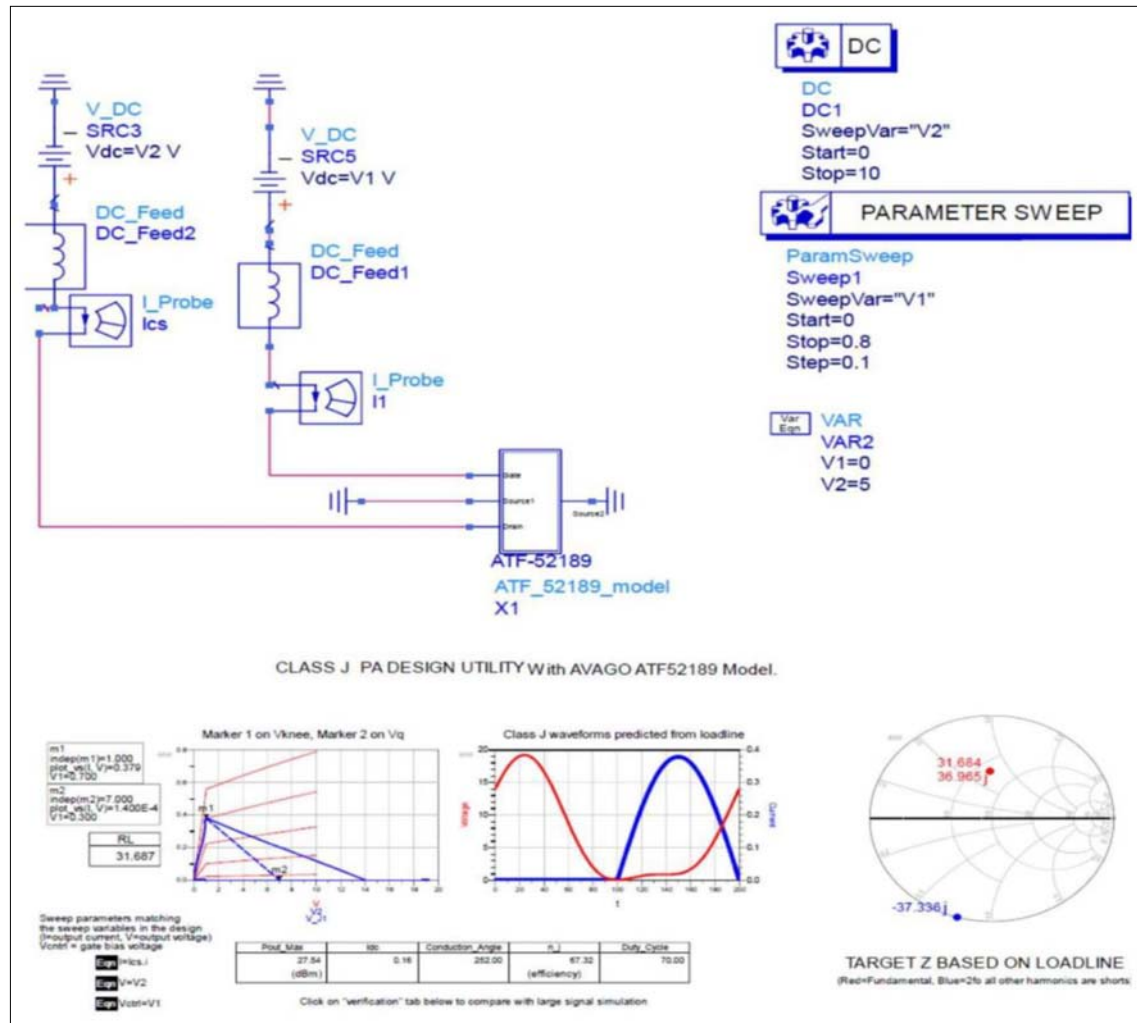


Fig. 5. DCIV characteristics schematic capture and class-J prediction

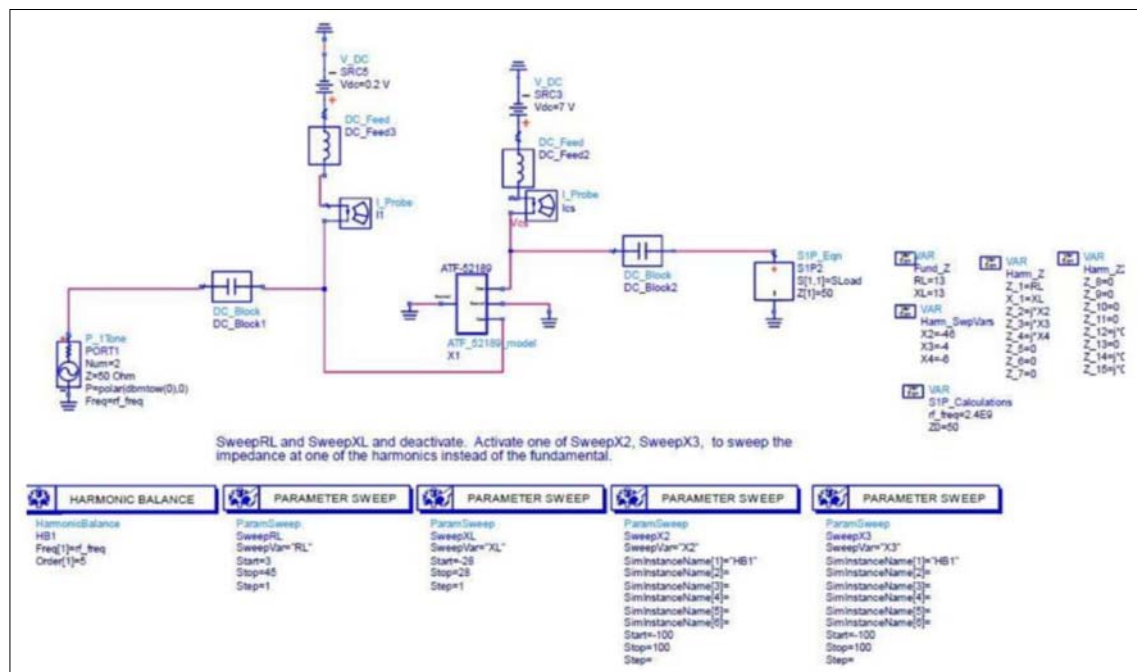


Fig. 6. Parasitic tune schematic and the swept parameters



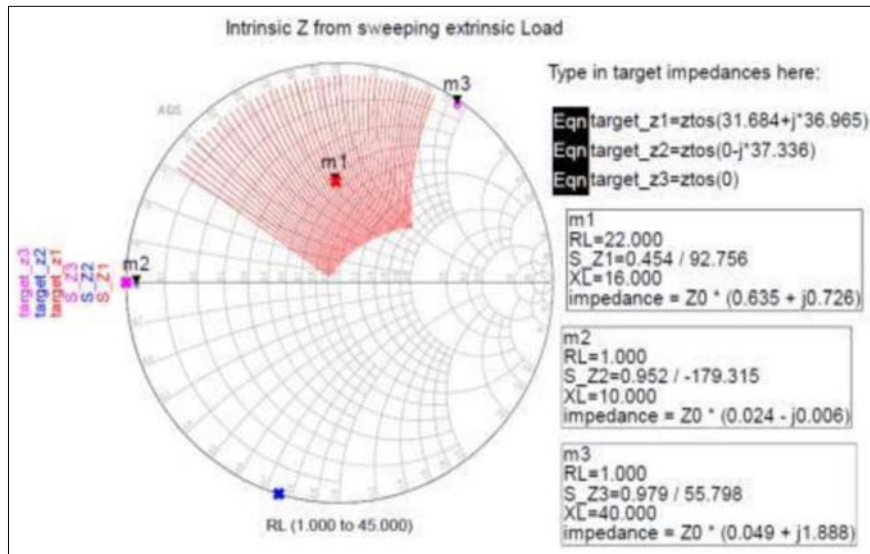


Fig. 7. Fundamental load tuning

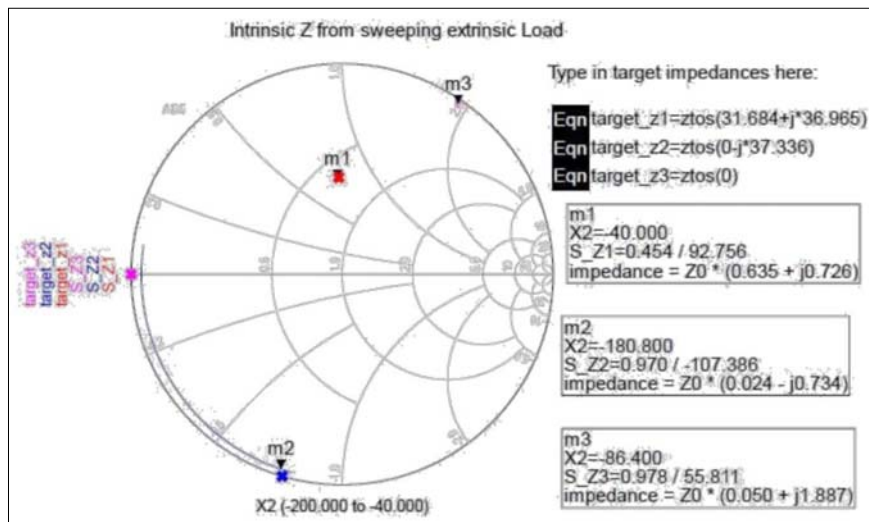


Fig. 8. Second harmonic tune

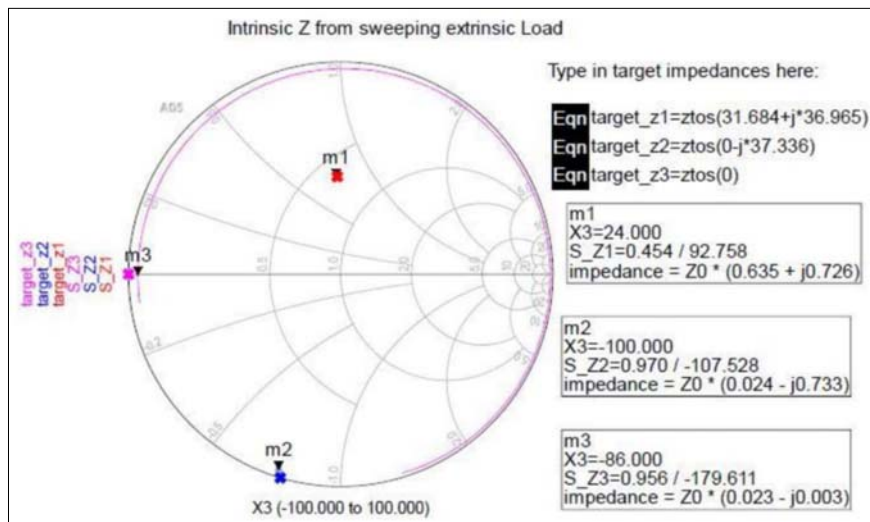


Fig. 9. Third harmonic tune

was adjusted so that the drain current swung over the whole DC load-line.

Figures 7–9 illustrate the data display for the swept impedances at fundamental, 2nd and 3rd harmonics.

The circuit schematic in Fig. 10 was used to determine the input impedance so that a conjugate matching network can be designed between the device and the driver.

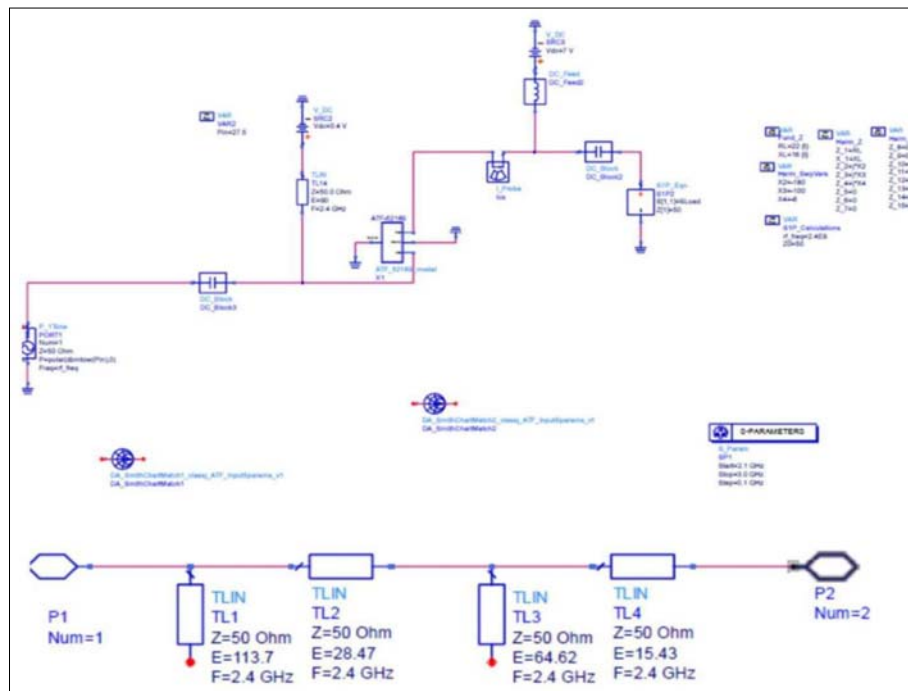


Fig. 10. Input impedance measurement and matching schematic

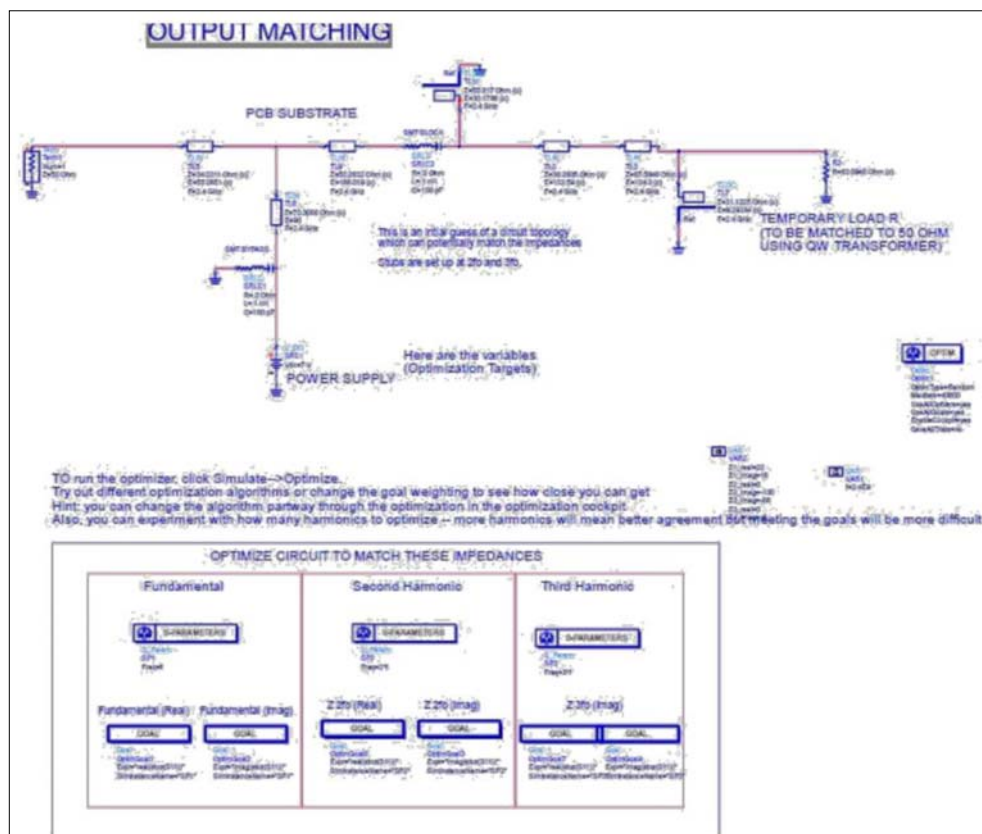


Fig. 11. Output impedance optimization schematic

### 2.5. Output network optimization

The external load obtained in the parasitic tune was approximated by the distributed element network illustrated in Fig. 11.

By defining the desired harmonic characteristics of the network as goals, the ADS optimization engine was used to fine tune each element within realizable

ranges so as to closely match the desired impedances. Figure 12 captures the optimization cockpit as it runs through 40 000 iterations.

### 2.6. Complete design simulation

The complete schematic design shown in Fig. 13 was simulated in order to compare its performance and waveforms with the load line prediction.

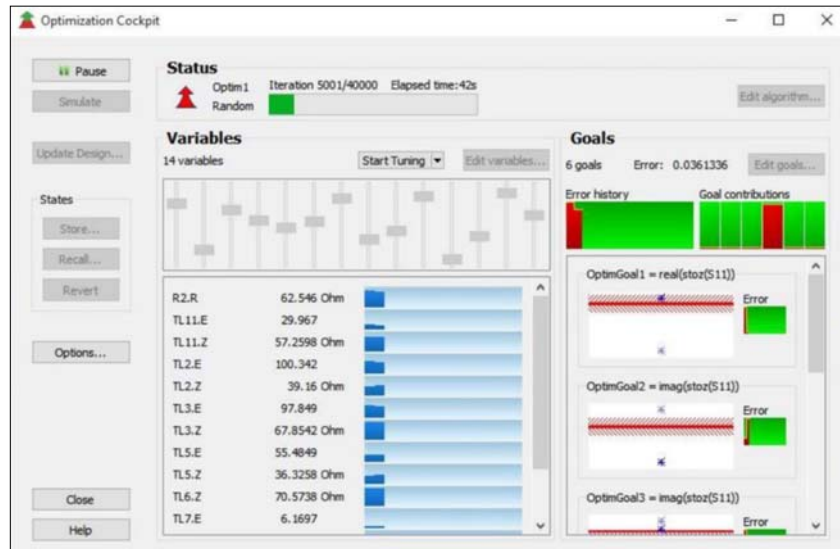


Fig. 12. Optimization in progress

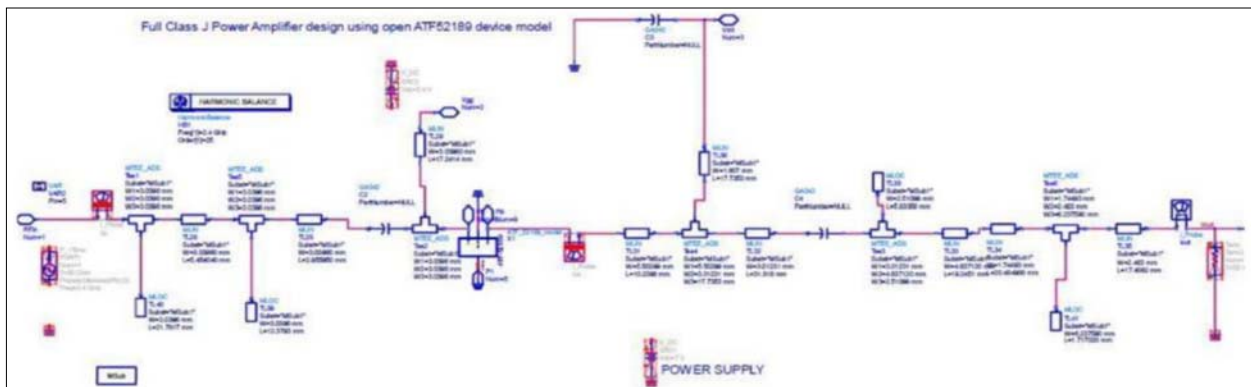


Fig. 13. Complete schematic design

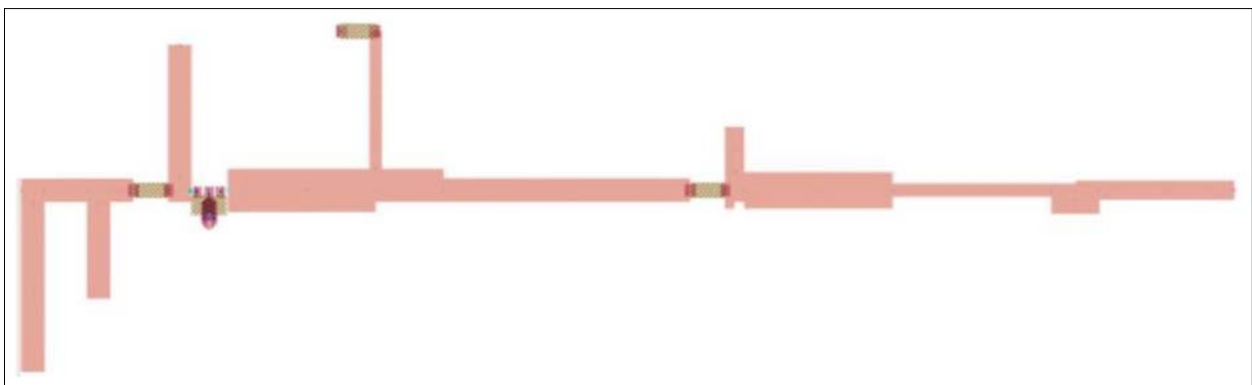


Fig. 14. 2.4 GHz layout design

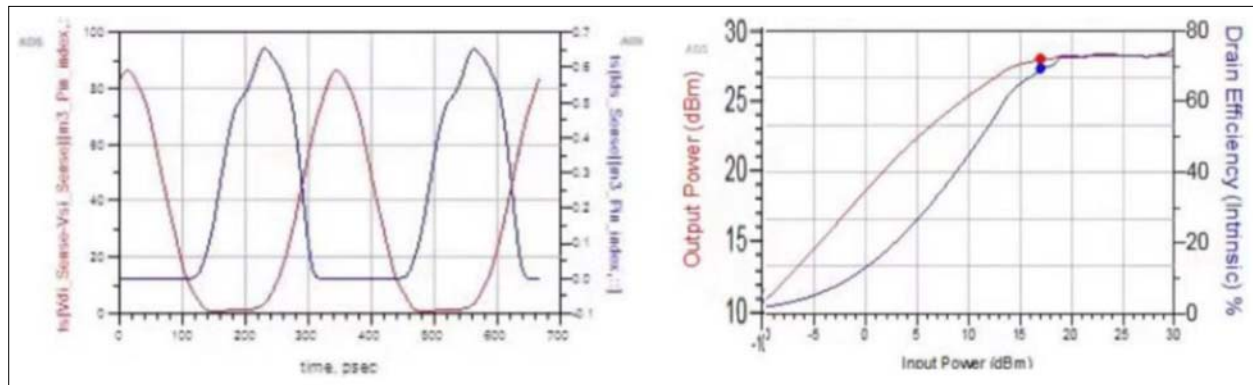


Fig. 15a. Simulated data display

Pout_predicted dBm	Pout_simulated dBm
23	21
Drain_efficiency_Predicted	Drain_efficiency_simulated
68.700	69.200

Fig. 15b. Simulation vs. prediction 2.4 GHz class-J PA

### 2.7. Layout design

The schematic design was converted into an FR4 substrate based layout design in readiness for fabrication. It was assumed that since the design was a simple single layer layout, EM simulation was not necessary. Figure 14 illustrates the layout design.

## 3. Simulation results

The simulation yielded the results illustrated in Fig. 15a and b. The power output and drain efficiency were almost matching the predicted values from the DC load-line.

## 4. Conclusion

The simulated 2.4 GHz PA closely achieved the predicted class-J waveforms, power output and efficiency performance. The slight discrepancy observed was attributed to the device parasitic other than the

output capacitance which was absorbed in the design. The output power designed for, 20 dBm, was slightly surpassed to yield a 21 dBm output.

## References

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